

Integration of a 5.5V BV_{CEO} SiGe HBT within a 200 GHz SiGe BiCMOS process flow

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Abstract — A novel BiCMOS integration scheme is described whereby high-performance, high breakdown-voltage SiGe HBTs can be integrated alongside ultra high performance, 200 GHz SiGe HBTs. The integration scheme is summarized and proof-of-concept data is shown to indicate the validity of the proposed scheme. It is shown that a 5.5V BV_{CEO} HBT with peak F_T of 45 GHz can be manufactured on the same wafer as a 200 GHz HBT with zero or one additional masking layers.

Index Terms — Silicon bipolar/BiCMOS process technology, power devices.

I. INTRODUCTION

In the past few years several manufacturers have presented SiGe BiCMOS process platforms that offer HBTs with cutoff frequencies greater than 200 GHz (see for example [1]-[3]). Fabrication of such devices requires the deposition of a thin ($< 0.5\mu\text{m}$ or so) epitaxial collector layer that sits on top of a highly-doped, buried subcollector. This thin collector deposition is necessary to reduce collector transit time and collector resistance in the device. However this thickness sets an upper limit on the breakdown voltage of any sibling HBT that is to be co-fabricated in the same technology. In 200 GHz technologies, the largest BV_{CEO} achievable on the same wafer seems to be in the 3-4V range [1]-[2].

A process which could co-integrate a 200 GHz HBT on the same wafer with a high-breakdown HBT would be valuable for many applications. For instance it would be well suited for future 100 Gigabit Ethernet (GbE) optical networks that require high speed and high voltage devices but require low cost integration to be viable [3]. A 4-channel 100 GbE implementation will transmit data at 25 Gbps and will require a combination of high density CMOS for the digital functions of the system with a 200 GHz HBT for the mixed signal elements on the receive end. Co-integrating a HV HBT on the same chip would allow the further integration of high speed electro-optic modulator drivers in the send circuitry which require 3V p-p operation.

In this work, it is shown that by creating separate collector configurations for the 200 GHz and

high-breakdown devices, nearly arbitrary BV_{CBO} and $BV_{CEO} > 5V$ can be achieved alongside a 200 GHz device.

II. PROCESS

The goal of this study was to fabricate a $> 5V$ BV_{CEO} device along side a manufacturable 200 GHz HBT. There are two obstacles to doing so: 1) as mentioned in the introduction, the epitaxial collector thickness necessary for achieving a robust 200 GHz HBT is such that the maximum BV_{CBO} possible for a device, even without any additional collector doping, is limited to 12V or so and 2) 200 GHz devices have extremely aggressive base profiles leading to high values of DC current gain (β). Since BV_{CEO} is dependent on both BV_{CBO} and (inversely related to) β , this makes achieving a device with $BV_{CEO} > 4.5V$ impossible if built on the same epitaxial collector as a 200GHz device.

Several studies have been made of implanted subcollector devices as a cost reduction method to replace the traditional buried subcollector / epi integration [4]-[6]. In all cases a penalty in collector resistance is to be expected. At the currents expected to be required for peak F_T in 200 GHz devices, the added collector resistance can pose an obstacle due to added collector voltage drop and added parasitic delays.

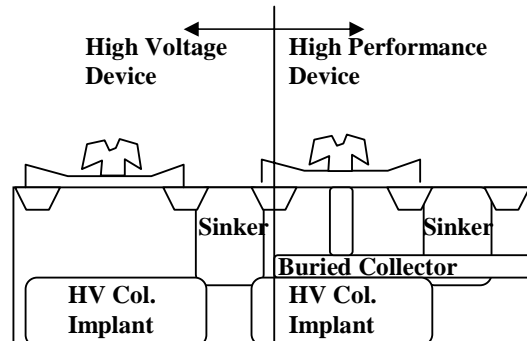


Fig. 1. Schematic of the construction of side by side 200 GHz and high-voltage devices.

However the implanted subcollector approach would seem to be ideally suited for less performance-demanding applications. As such it is proposed that a

traditional, high performance, buried-collector HBT be fabricated along side an implanted-collector high voltage HBT to achieve the best of both worlds. The devices used in this study are based on the Jazz SiGe200 SiGe BiCMOS process, the details of which can be found in [7]. Schematics of the high-performance and high-breakdown devices are shown in Fig. 1. In the usual 200 GHz process, every SiGe HBT has the buried subcollector implant mask layer drawn over the whole device area. This implant was intentionally skipped on some wafers to form high voltage devices. Shallow trench isolation was then fabricated followed by a collector sinker implant, then standard CMOS processing steps. After the CMOS spacer was deposited a masking layer was used to clear out the spacer in the NPN areas. In the new process flow this etch-mask layer was changed to be a thick photoresist process and was simultaneously used as an implant mask for the implanted subcollector. In “HV” devices this implant alone formed the subcollector. In high speed devices, this implant merely added to the background of the already highly-doped collector region.

Various deep collector doses were evaluated to achieve a range of breakdown values. While one could theoretically produce devices with arbitrary BV_{CBO} by making the HV subcollector implant deeper or of a lower dose, in this study it was decided to stay within a few practical limits: 1) The dose should be such that the subcollector resistance does not begin to degrade simple DC characteristics such as premature roll over of the gummel plot or poor knee voltage in output characteristics and 2) The combination of dose and energy had to be such that it avoided amorphization or significant damage of the silicon since there is little thermal budget left to heal the silicon lattice at this stage in the process. The data shown below is all for a case that meets these requirements but still achieves a BV_{CEO} comfortably greater than 5V.

III. DC RESULTS

Figure 2 shows a gummel plot, output curves along with a base current reversal plot, base collector reverse bias diode breakdown plots, and a comparison of I_C for single and arrayed devices, all for a HV device. Figure 2 (a) shows ideal behavior over several orders of magnitude of I_C . Further it shows that the added collector resistance does not interfere with the operation of the device near the I_C required to achieve peak F_T , which may or may not be true for 200 GHz devices fabricated with implanted subcollectors. Figure 2 (b) shows output characteristics overlaid with a base current reversal plot, sharing the same abscissa. It can be seen that either the direct method of obtaining BV_{CEO} from the

output curves or the inferred method from base current reversal yield similar results of 5.5 V or greater. Also note the very weak dependence of knee voltage on collector current which again suggests that collector resistance is not severely impacting this device’s performance. Figure 2 (c) shows base-collector avalanche breakdown occurring at $> 16V$; much more than could be achieved with the standard 200 GHz process buried subcollector. Figure 2 (d) shows that, for a 200-device array, the collector current scales nearly perfectly with number of devices over several orders of magnitude, indicating excellent device matching.

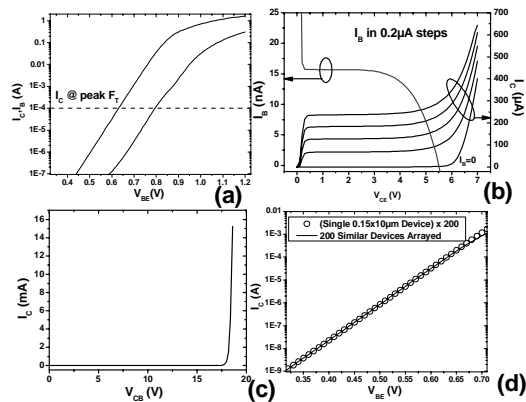


Figure 2. (a) Gummel plot. (b) Output curves with base current reversal plot overlaid. The left ordinate is base current and the right ordinate is collector current. (c) Base-Collector reverse bias diode characteristic showing $>16V$ BV_{CBO} . (d) Comparison of I_C of a single $0.15 \times 10 \mu m$ device multiplied by 200 with I_C of 200 such devices arrayed in parallel.

In order to further illustrate the manufacturability of this process, all-die wafer maps were performed. Figure 3 shows plots of BV_{CBO} vs. BV_{CEO} of the HV device for all die on one wafer. It is seen that BV_{CBO} is very tightly controlled, perhaps even more so than for buried collectors since the variation in BV_{CBO} for this process is dependent on implant uniformity rather than epitaxial uniformity. Indeed when a single outlier (not shown) was removed from the data, the within-wafer 3σ variation of BV_{CBO} is less than 0.4V and less than 0.6V for BV_{CEO} .

IV. RF RESULTS

RF measurements were taken both on the HV and high performance devices as well as on high-performance devices fabricated from control wafers within the same lot. Figure 4 shows an F_T - J_C plot of the HV device. The data shows a peak F_T of 45 GHz which suggests an excellent $F_T \times BV_{CEO}$ product of nearly 250 GHz-V. Further, and perhaps more importantly, the device exhibits a slow degradation in

F_T as one moves to lower values of J_C due to low parasitic capacitances. F_T is still as high as 24 GHz at $0.1 \text{ mA}/\mu\text{m}^2$. An F_{MAX} of 130GHz was observed at the J_C required for peak F_T .

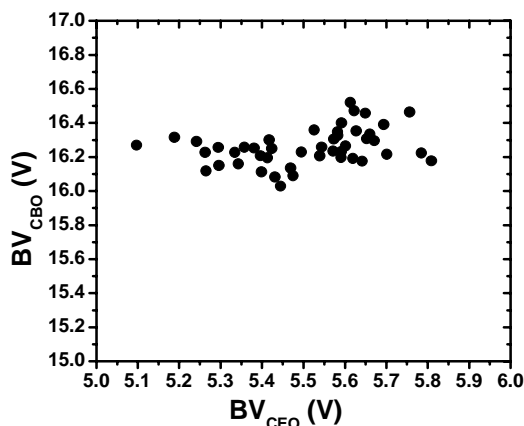


Figure 3. All-site BV_{CBO} vs BV_{CEO} data for the HV device

Figure 5 shows the F_T - J_C plots of two high performance devices, one control and one that received the HV collector implant in addition to the usual collector implant. This device represents the “zero mask-adder” approach since one could non-selectively implant the HV collector in every HBT, not just the HV HBTs, thus creating the new HV device without adding any masking layers. As can be seen in the plot, adding the HV implant does degrade the performance slightly, producing a peak F_T penalty of about 6 GHz. The F_{MAX} is degraded more, by about 10 GHz, due to increased C_{BC} . DC characteristics showed no obvious differences. Nevertheless, it is clear that without adding any masks a 200 GHz F_T HBT can be fabricated on the same wafer as a 5.5V BV_{CEO} HBT. With one additional mask, the 200 GHz device performance can be preserved entirely and the HV implant can be performed in an earlier stage in the process where more thermal budget is available to heal implant damage.

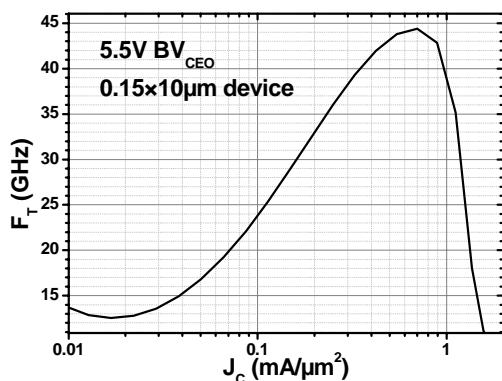


Figure 4. F_T vs J_C plot for the 5.5V BV_{CEO} device. Note the high F_T values at low current densities.

If the one mask-adder approach is applied (ostensibly making the 200 GHz HBT completely independent of the HV integration), there is an opportunity to customize the HV collector profile. Figure 6 shows an F_T - BV_{CEO} scatter plot for HV devices built with many different collector doses and energies. The devices are divided into two groups. The first (filled circles) represents an integration scheme where the high energy HV collector implant is done at the beginning of the process flow, just after the buried layer implant is done for the high performance device. The idea with this group was to allow arbitrary thermal budget to fully activate the implanted collector dose and fully heal whatever lattice damage that might be caused by the high energy implantation. The second group was processed as described above, after the CMOS is formed and before the SiGe base is deposited. It seems that the group with the early collector implant performs better at lower breakdown but actually gets worse from an $F_T - BV_{\text{CEO}}$ standpoint as the collector dose is decreased. On the other hand the group with the collector implant done later seems to improve in $F_T \times BV_{\text{CEO}}$ as the collector dose is decreased. The difference must be attributed to the shape of the profile; more diffused in the first group and sharper in the second group. This is an interesting finding in and of itself with regards to collector engineering of high breakdown SiGe HBT devices regardless of how they are constructed.

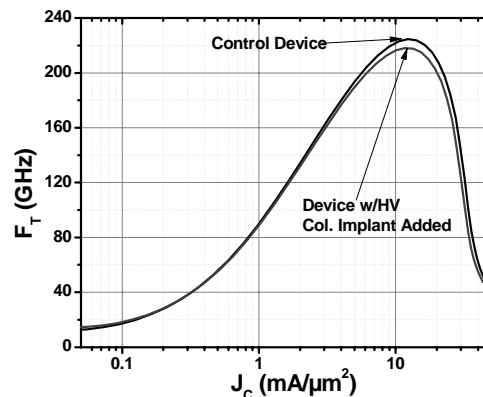


Figure 5. F_T vs. J_C plot for the high performance HBT with and without the HV collector implant.

Finally, Figure 7 shows the HV device against the competitive landscape for some other high-breakdown SiGe HBT processes currently in production. It can be seen that the devices fabricated for this study compare favorably with any of the other devices currently available and they are the only ones that can

be readily integrated with a manufacturable 200 GHz HBT.

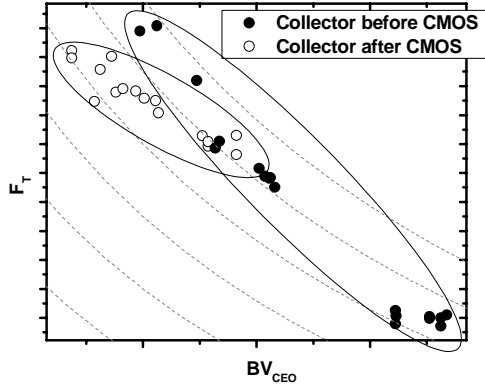


Figure 6. F_T vs. BV_{CEO} plot for HV devices with several different collector implants. The filled circles represent data for devices where the collector implant was performed before the significant thermal budget steps in the process. The open circles represent data for devices where the collector implant was performed after most thermal budget steps had already been completed.

V. CONCLUSION

A 5.5V BV_{CEO} HBT with $F_T \times BV_{CEO}$ product of 250 GHz \times V has been fabricated in an integration scheme fully compatible with state of the art 200 GHz HBTs. This device can be integrated without adding a mask with only a very small penalty to the 200 GHz device performance or with no affect on device performance if one mask is added. On its own merits, the new device performs comparably or better than other high-breakdown devices currently offered in the industry.

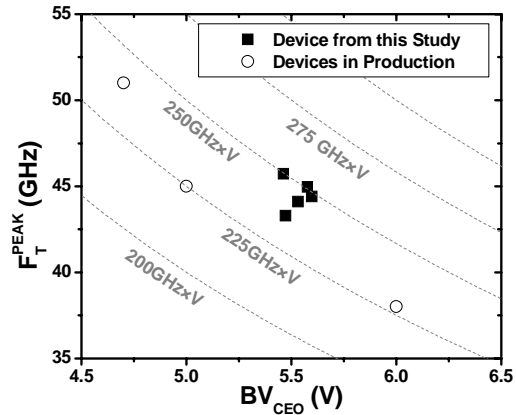


Figure 6. F_T vs BV_{CEO} plot for the devices described in this study along with several currently available commercial high voltage HBT devices.

REFERENCES

- [1] B. A. Orner, et al., *2003 IEEE BCTM Proceedings*, 11.2, pp 203-206, 2003.
- [2] J. Böck et al., *2004 IEEE BCTM Proceedings*, 4.2, pp 84-87, 2004.
- [3] G. Oulunsden and R. Lingle, *IEEE 802.3 Higher Speed Study Group Meeting Minutes*, March 2007. Available at <http://grouper.ieee.org/groups/802/3/hssg/public/mar07/index.html>
- [4] M. Miura et al., *IEEE Trans. Electron Dev.*, vol. 53, issue 4, pp 857-865, April 2006.
- [5] L. Lanzerotti et al. *2004 IEEE BCTM Proceedings*, 12.4, pp 237-240, 2004.
- [6] B. Heinemann et al., *2003 IEEE IEDM Proceedings*, pp 775-778, 2003.
- [7] P. Chevalier et al., *2005 IEEE IEDM Proceedings*, 38.6, pp 963-966, 2005.
- [8] M. Racanelli et al., *2001 IEEE IEDM Proceedings*, pp 336-339, 2001.