SEMICONDUCTOR

MOSVAR
PSP Based
MOS Varactor Model

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Outline

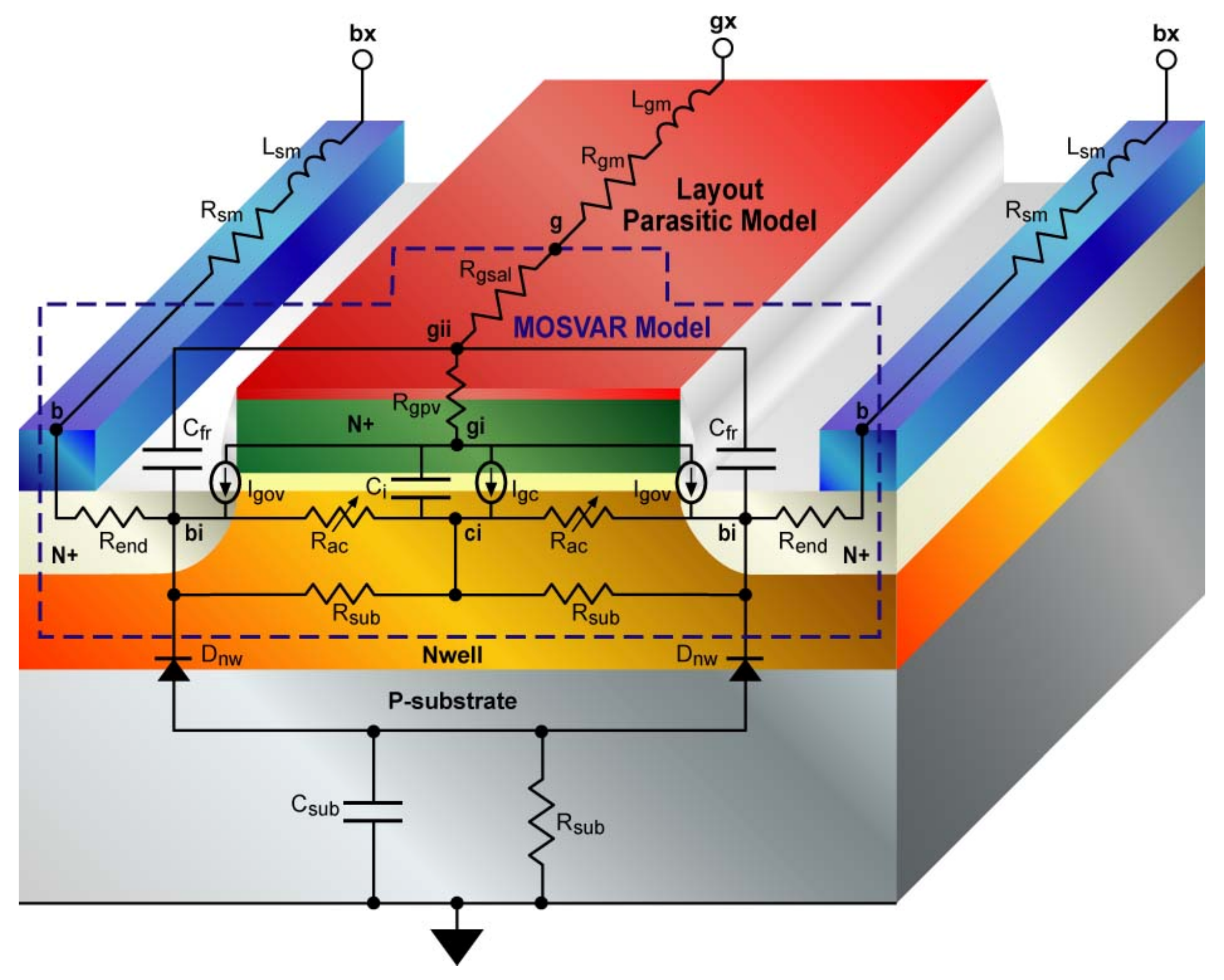
- Motivation
- MOSVAR: Industry Standard PSP Based MOS Varactor Model
- Critical Discussion on MOS varactor influence on VCO design

Motivation for CMC Standard Model

- MOS Varactor is typically only tuning element in RFCMOS PDKs
  - Multiple voltage range devices offered based on Tox levels
- Clear need for model meeting CMC high standard for model quality
- CMC MOSVAR Subcommittee formed in April 2006, model developed by Victory, Yan, Gildenblat, McAndrew, Anderson, et. al., chosen as base (EDL May 2001, TED August 2005)
- Model code unified with PSP model wherever possible
  - Provides natural consistency and statistical harmony between MOS devices in process
  - New gate current formulations derived since poly-well configurations different in MOS varactor
- Model available now to CMC members in verilogA and shared libraries in spectre
- CMC standardization set for October 2007
  - EDA vendor implementation underway

MOS Varactor

- Intrinsic C generated from frequency dependent surface potential formulation
- Scalable parasitic models ensure accurate CV and Quality Factor (Q) simulation
- Physical Gate Current models critical for 130nm and below technologies
- Layout parasitics, substrate network part of extrinsic model



MOSVAR Model Parameters: PSP harmonization

Parameter	Description
TOXO	Oxide thickness
VFBO	Flatband voltage
NSUBO	Substrate (Well) doping level
NPO	Polysilicon doping level
QMC	Quantum mechanical correction factor
DLQ	Length delta for intrinsic capacitance
DWQ	Width delta for intrinsic capacitance
DWR	Width delta for substrate resistance
NGCON	Number of gate contacts (1 or 2)
TAU	Time constant for inversion charge recombination/generation
CFRL	Fringing capacitance in length direction
CFRW	Fringing capacitance in width direction
RSHG	Gate sheet resistance
RPV	Vertical poly contact resistance
REND	End resistance/unit width
RSHS	Substrate (Well) sheet resistance
UAC	Accumulation layer zero bias mobility
UACRED	Accumulation layer mobility reduction factor
STVFB	Temperature exponent of VFB
STRSHG	Temperature exponent of RSHG
STRPV	Temperature exponent of RPV
STREND	Temperature exponent of REND
STRSHS	Temperature exponent of VFB
STUAC	Temperature exponent of UAC
NOVO	Doping of overlap region
LOV	Length of overlap region
GCOO*	Gate tunneling energy adjustment
IGINVLW*	Gate channel current pre-factor
IGOVW*	Gate overlap current pre-factor
STIG*	Temperature coefficient for iginv and igov
GC2O*	Gate current slope factor
GC3O*	Gate current curvature factor
CHIBO*	Tunneling barrier height

Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (1)

- Inversion charge in MOS capacitor thermally generated, not supplied by source/drain regions as in MOSFET
- Full solution requires inclusion of continuity equations, not practical for circuit simulation
- Inversion charge relaxation time approximation provides reasonable physical model suitable for circuit simulation
- Important for VCO design where DC biasing in inversion, allowing inversion charge to form, will change the frequency response
  - Different than DC biasing in depletion with RF signal swinging into inversion region, inversion charge has no time to form

Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (2)

$$\frac{dq_i}{dt} = \frac{q_i^{(0)} - q_i}{\tau}$$

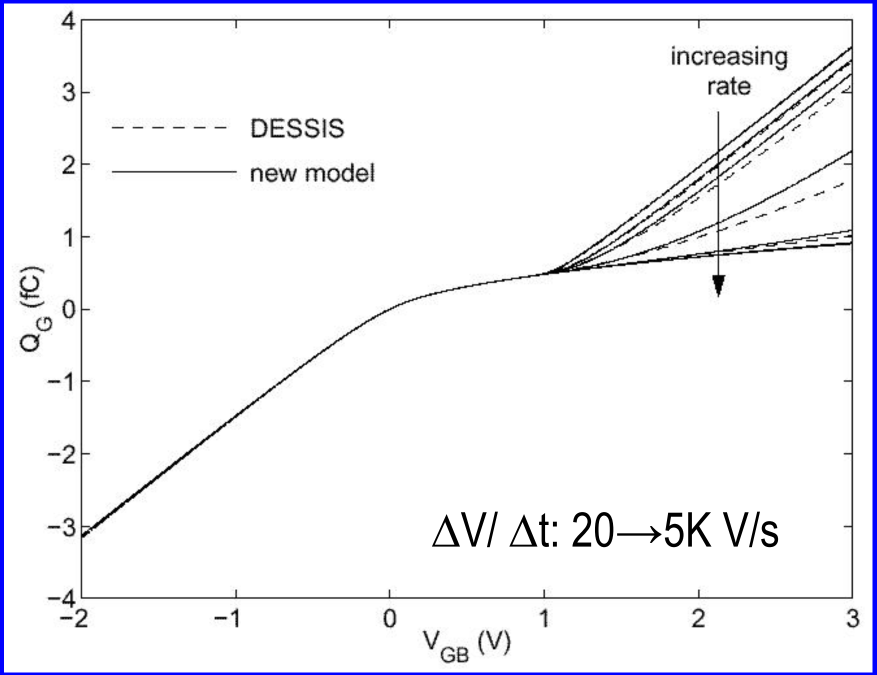
Inversion charge (normalized) relaxation equation,
$q_i^{(0)}$: static inversion charge generated from static analytical surface potential

$$[V_{GB}(t) - V_{FB} - \psi(t) - q_i(t)]^2 = \gamma^2 \Phi_t [u - 1 + \exp(-u)]$$

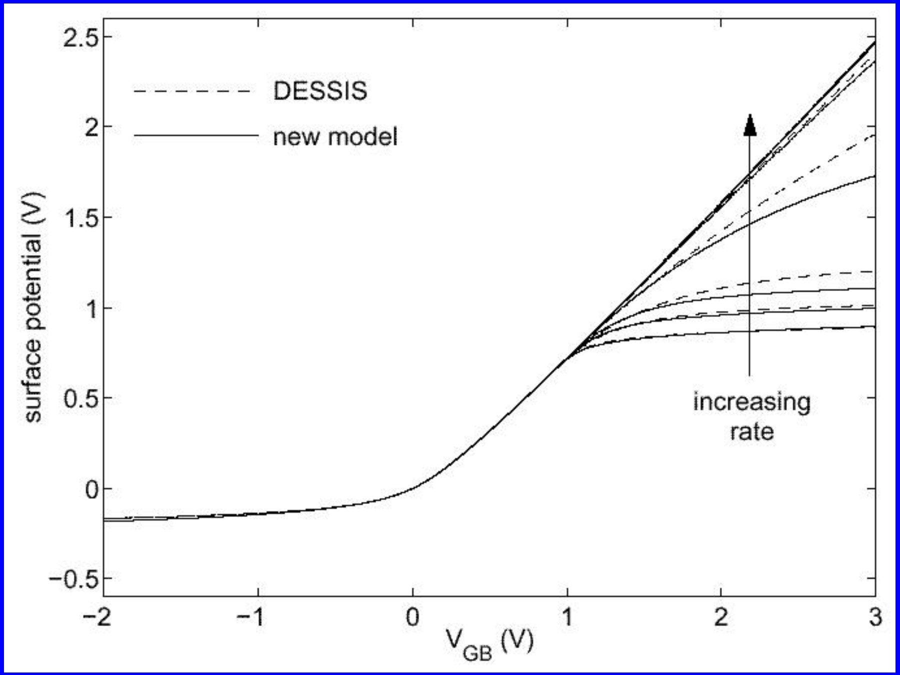
Time dependent surface potential equation

$$u = \frac{\psi(t)}{\Phi_t}$$

normalized surface potential

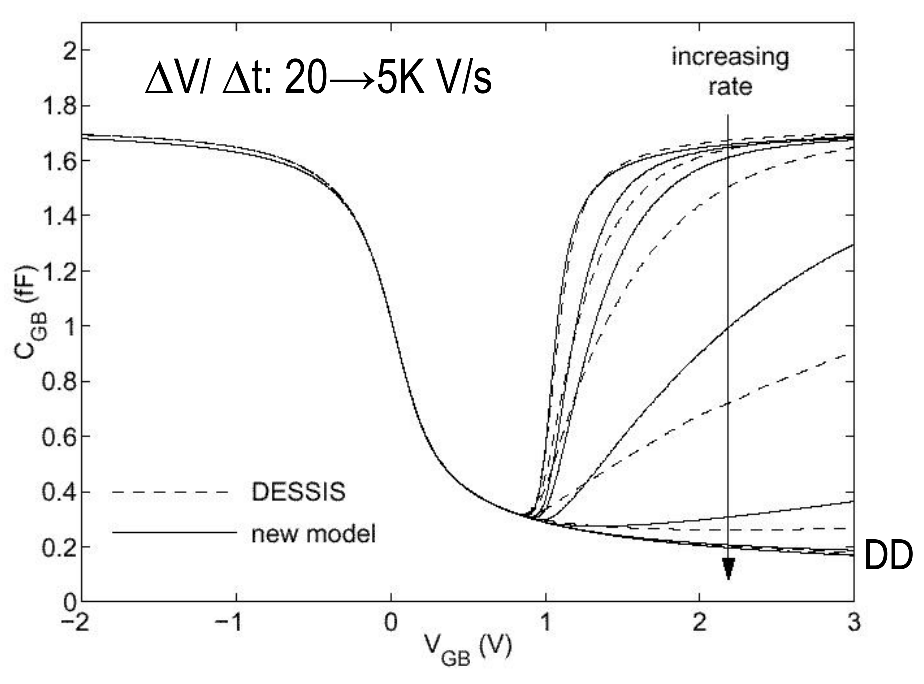


ΔV/ Δt: 20→5K V/s

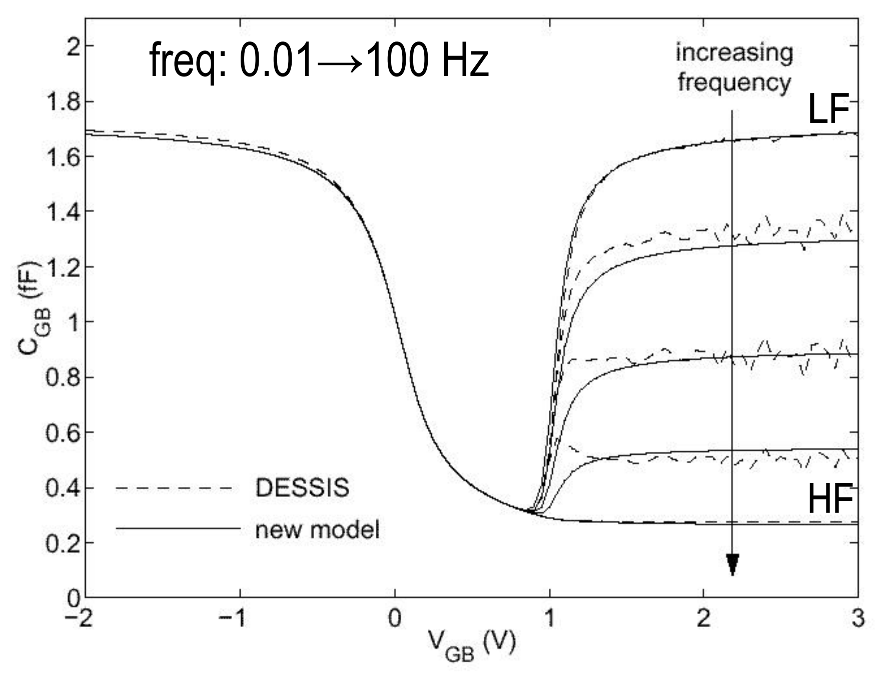


Frequency Dependent Analytical Surface Potential Based MOS Capacitance Model (3)

Transient



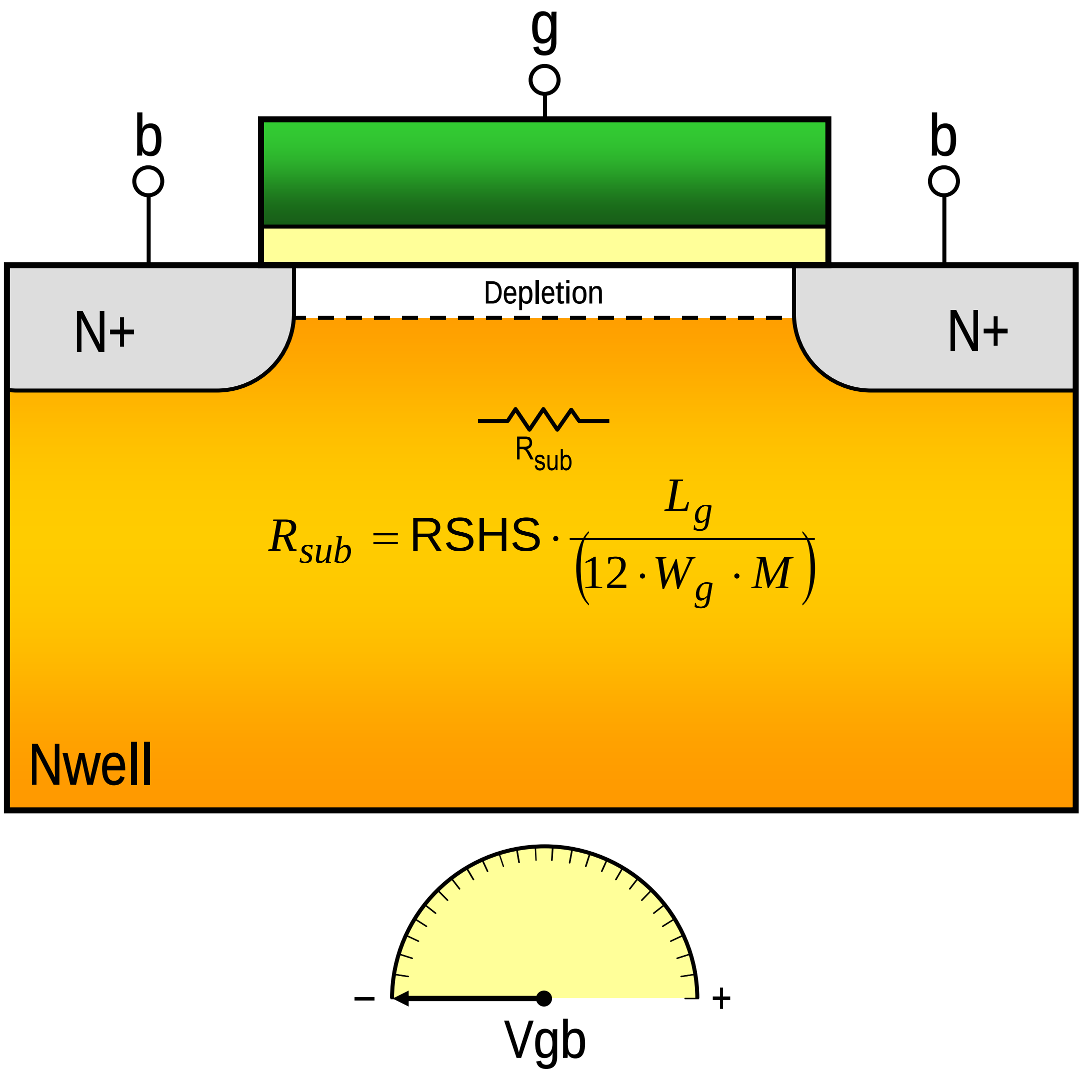
AC



Bias Dependent Well Resistance

- Depletion width small due to high doping
- Negligible compared to Well thickness
- Ignore voltage dependence of R_{sub}

- Accumulation Charge Q_{ac} calculated directly from surface potential
- Voltage dependent surface scattering included in mobility μac_v



$$R_{sub} = \mathrm{RSHS} \cdot \frac{L_g}{\left(12 \cdot W_g \cdot M\right)}$$

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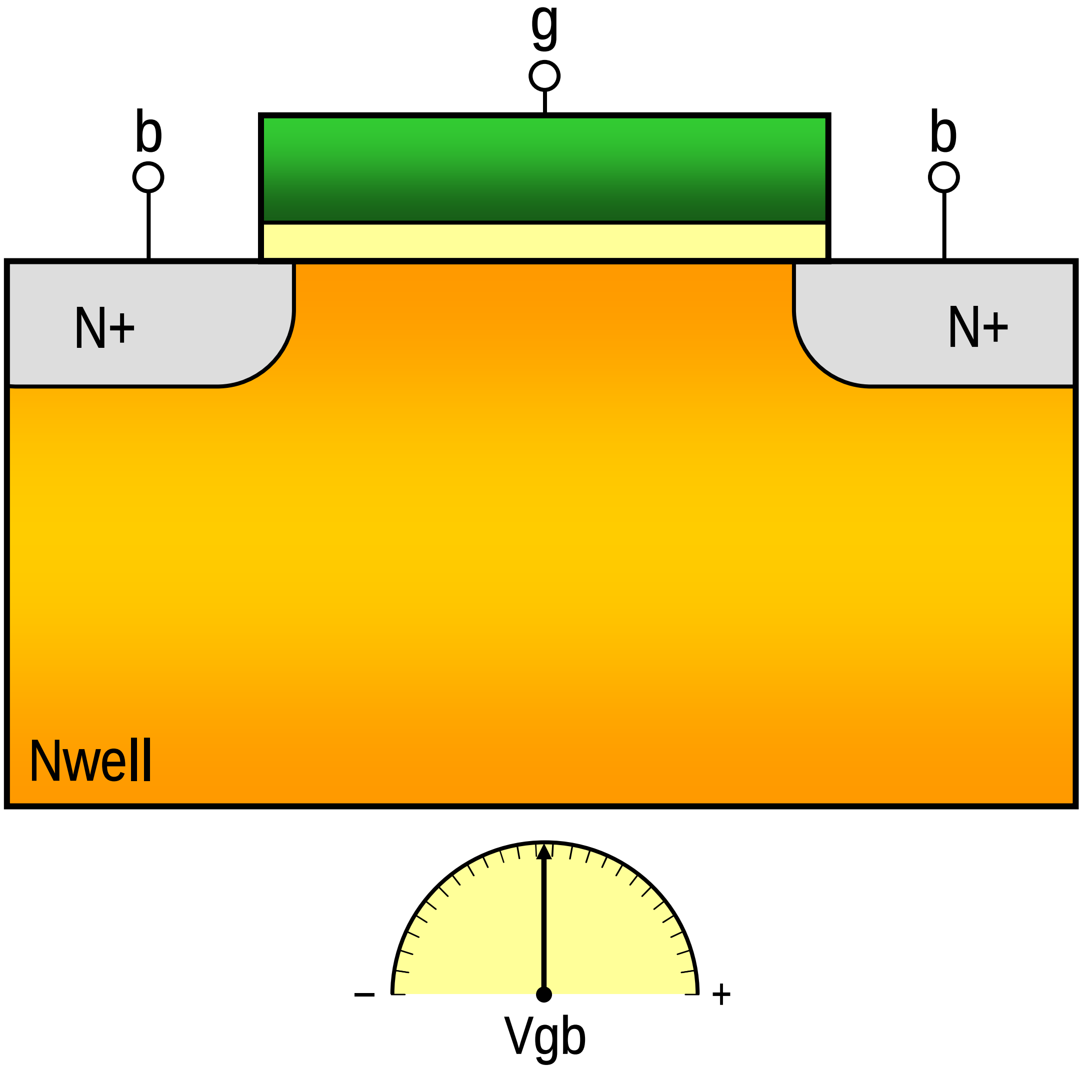

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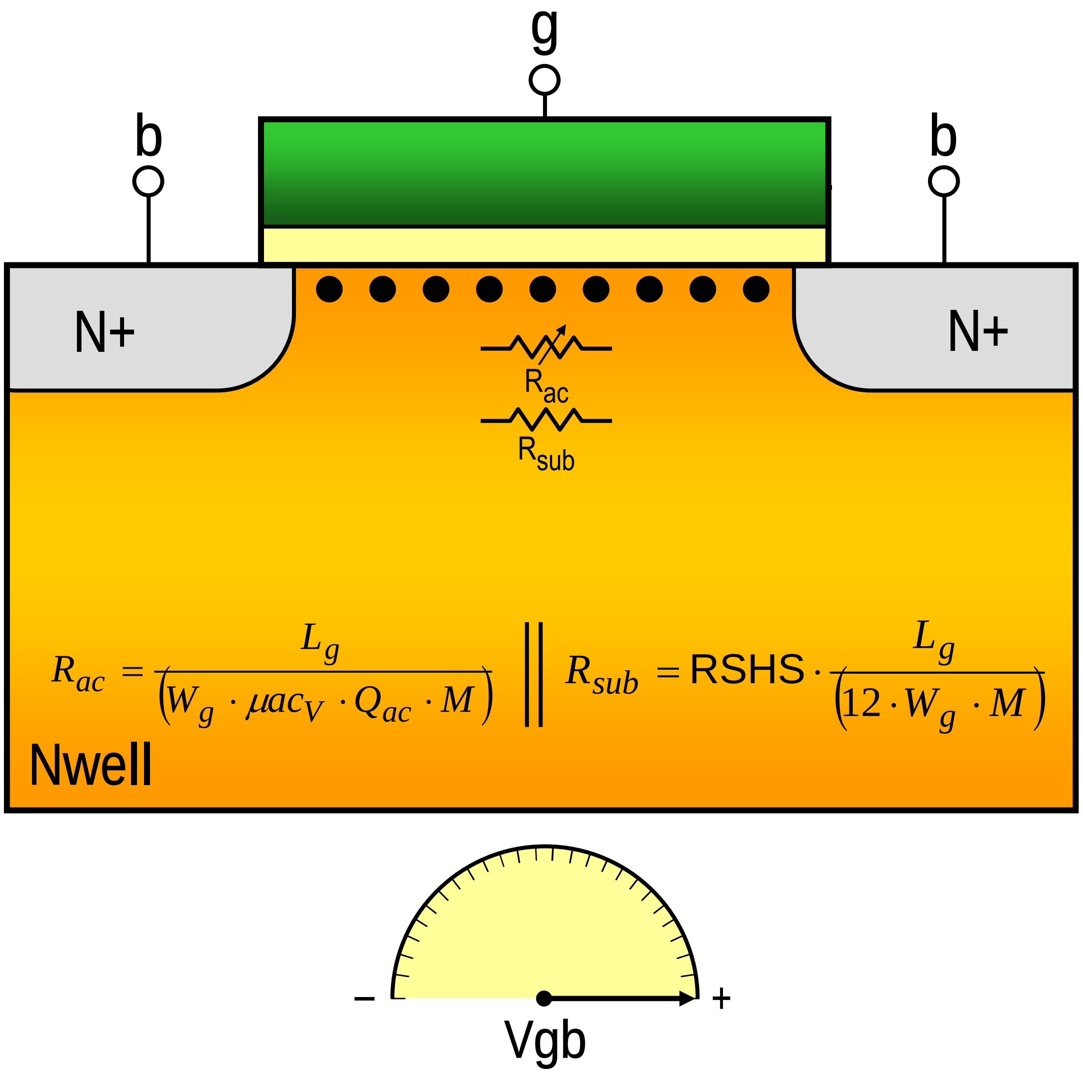
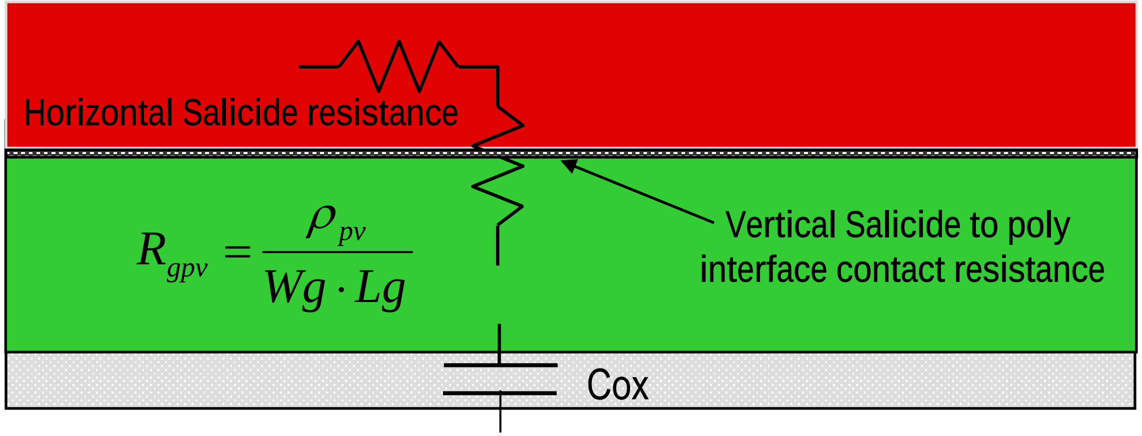


$$R_{ac} = \frac{L_g}{\left(W_g \cdot \mu ac_V \cdot Q_{ac} \cdot M\right)} \quad \Big\| \quad R_{sub} = \text{RSHS} \cdot \frac{L_g}{\left(12 \cdot W_g \cdot M\right)}$$

Poly Gate Resistance Model

- Includes salicide to bulk poly contact resistance – vertical component
  - Dominant component of Rgate at narrower widths, short lengths
- Accurate modeling of Rg scaling

$$R_{gsal} = \frac{\rho_{sal} \cdot Wg}{Lg \cdot 3 \cdot N_{cnts}^{2}}$$



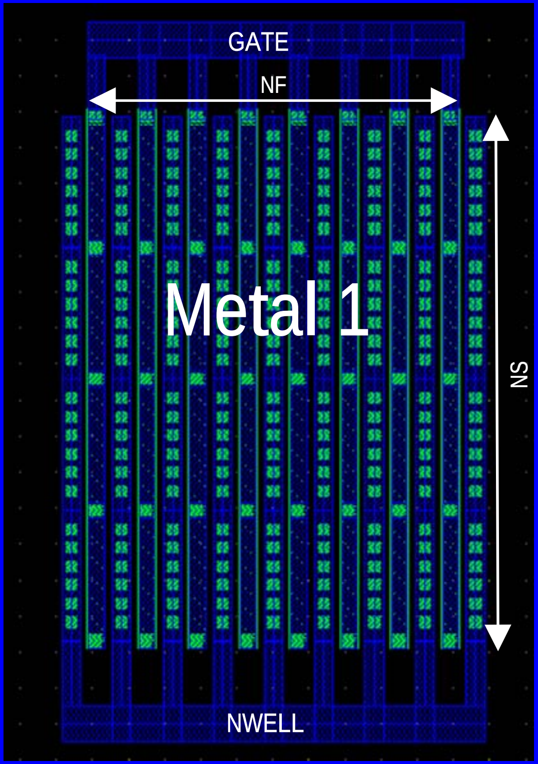
Horizontal Salicide resistance

$$R_{gpv} = \frac{\rho_{pv}}{Wg \cdot Lg}$$

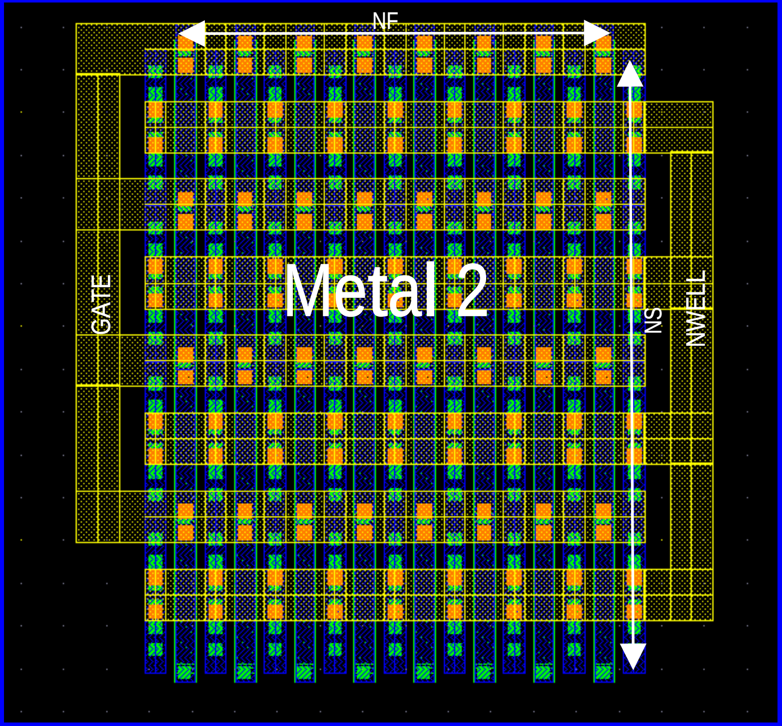
Vertical Salicide to poly interface contact resistance

Cox

MOS Varactor Layout and Metal Connection Considerations



vs.



- Metal R and L ~ NS/NF (segments)
- High metal resistance (thin M1)
- Low metal capacitance (M1-M1)

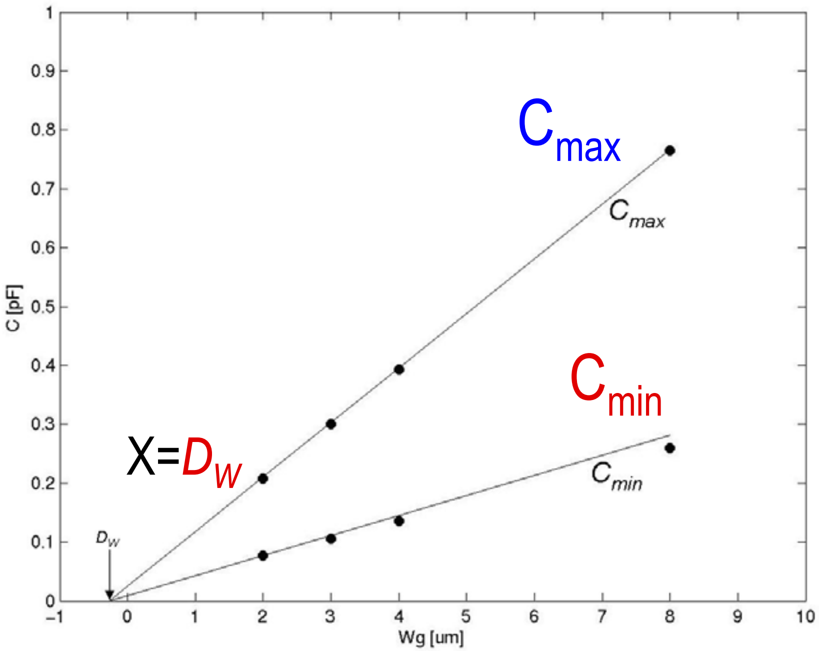
- Metal R and L ~ NF/NS (fingers)
- Low metal resistance (wide M2)
- High metal capacitance (M2-M1)

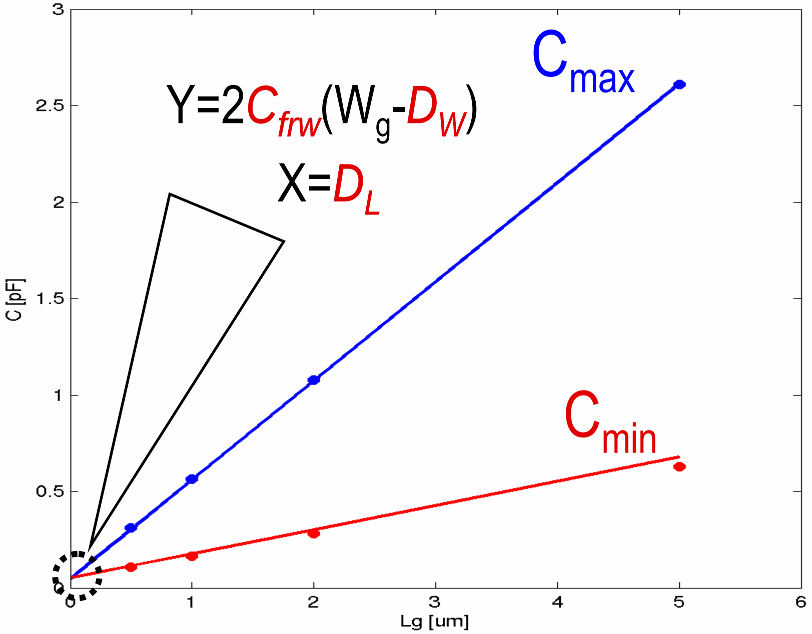
Physical Parameter Extraction: Scalable MOS Capacitance

- Regression fitting of C_{max} and C_{min} on W_g and L_g yields D_L, D_W, C_{frw}
- T_{ox}, N_b (well doping), QM, and PD parameters extracted from large plate capacitor

$$C_{max} = \left(C_{ox}\cdot\left(L_g - D_L\right)\cdot\left(W_g - D_W\right) + 2C_{frw}\cdot\left(W_g - D_W\right)\right)\cdot\left(N_s\cdot N_f\right)$$

$$C_{min} = \left(\frac{C_{ox}\cdot C_{dep}}{C_{ox} + C_{dep}}\cdot\left(L_g - D_L\right)\cdot\left(W_g - D_W\right) + 2C_{frw}\cdot\left(W_g - D_W\right)\right)\cdot\left(N_s\cdot N_f\right)$$

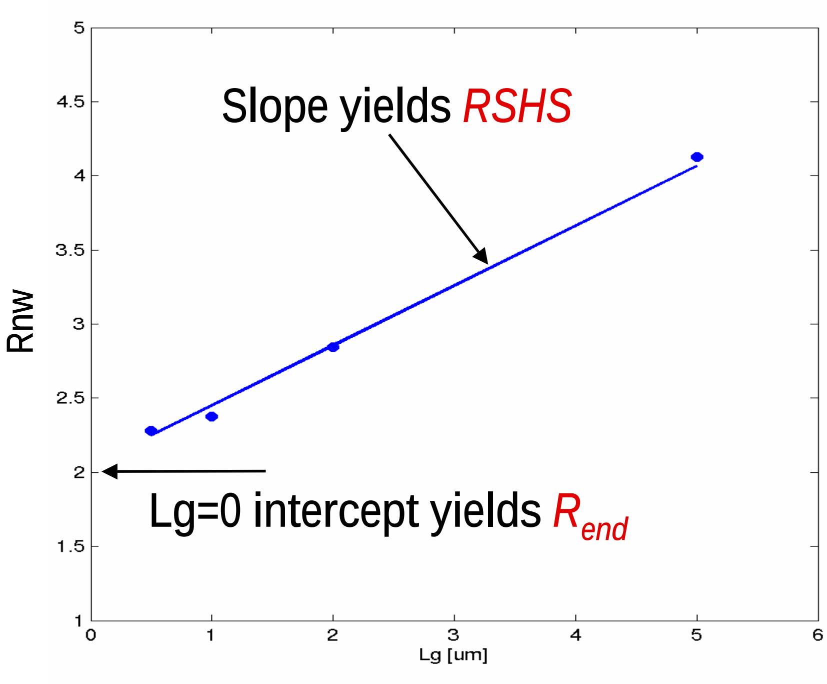




Scalable Nwell Resistance Model Extraction

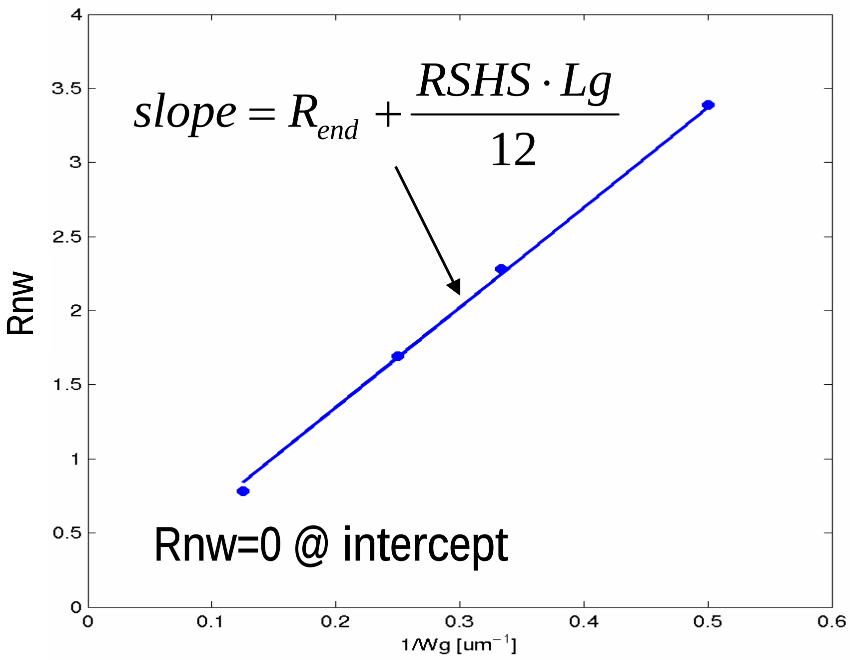
$$R_{nwell} = \frac{R_{end}}{Wg} + \frac{RSHS \cdot Lg}{Wg \cdot 12}$$

- Physical extraction through regression vs. Lg
- Plot vs. 1/(Wg) verifies model accuracy



Slope yields *RSHS*

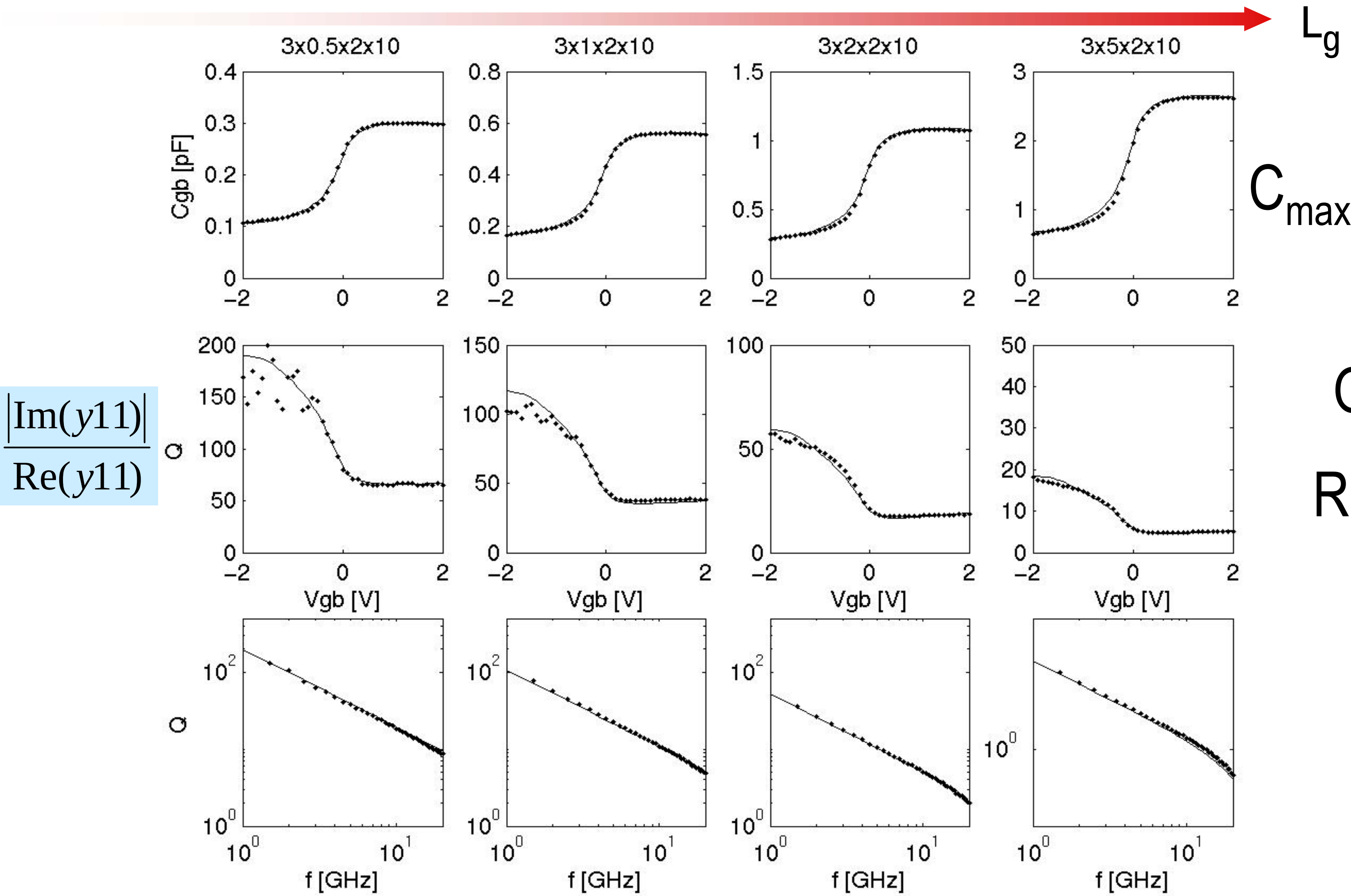
Lg=0 intercept yields R_{end}



$$slope = R_{end} + \frac{RSHS \cdot Lg}{12}$$

Rnw=0 @ intercept

MOS Varactor Model Results: Varying Lg (0.18 RFCMOS 1.8V Device)



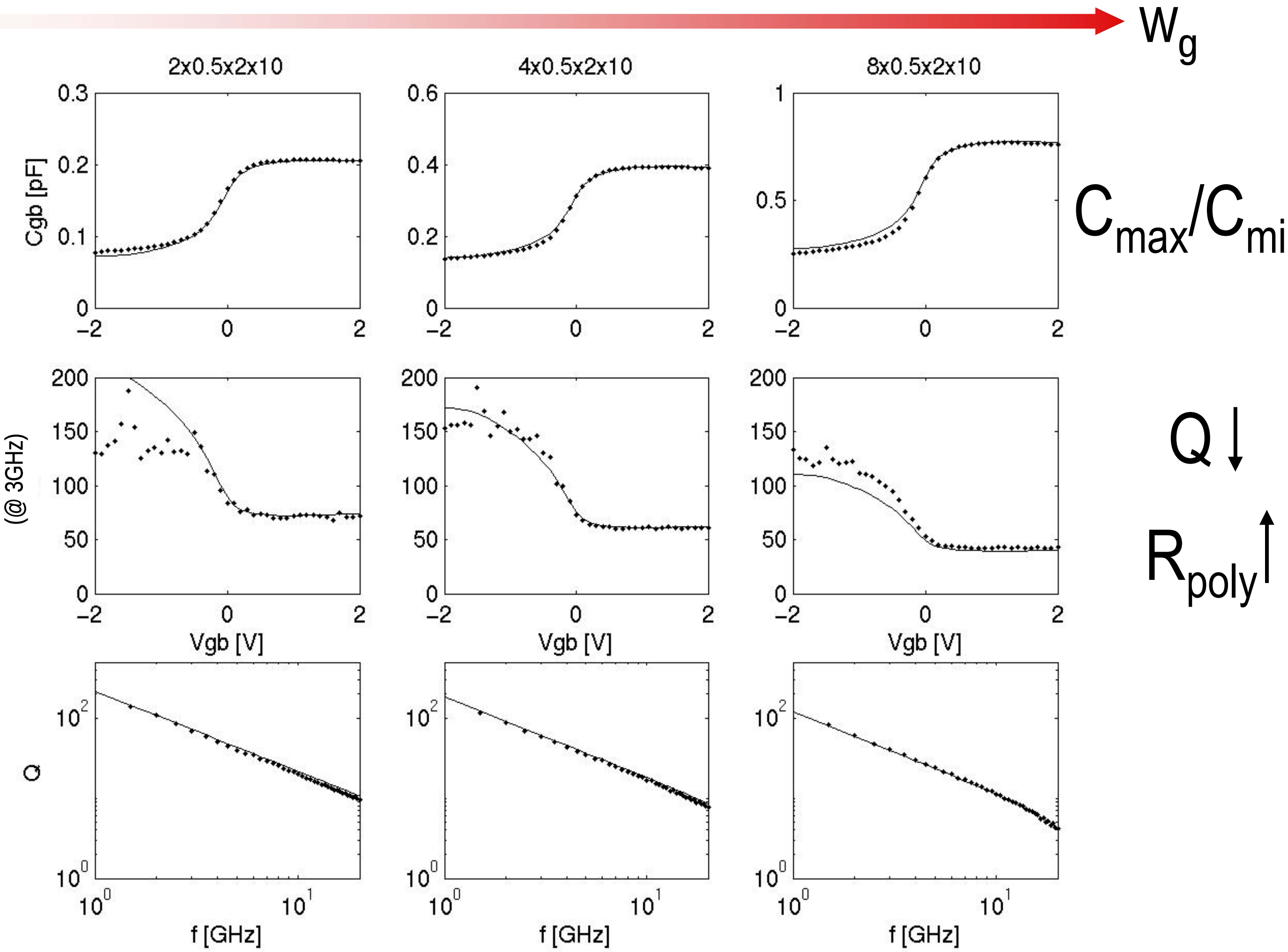
$$Q = \frac{|\mathrm{Im}(y11)|}{\mathrm{Re}(y11)}$$

C_{max}/C_{min} ↑

Q ↓

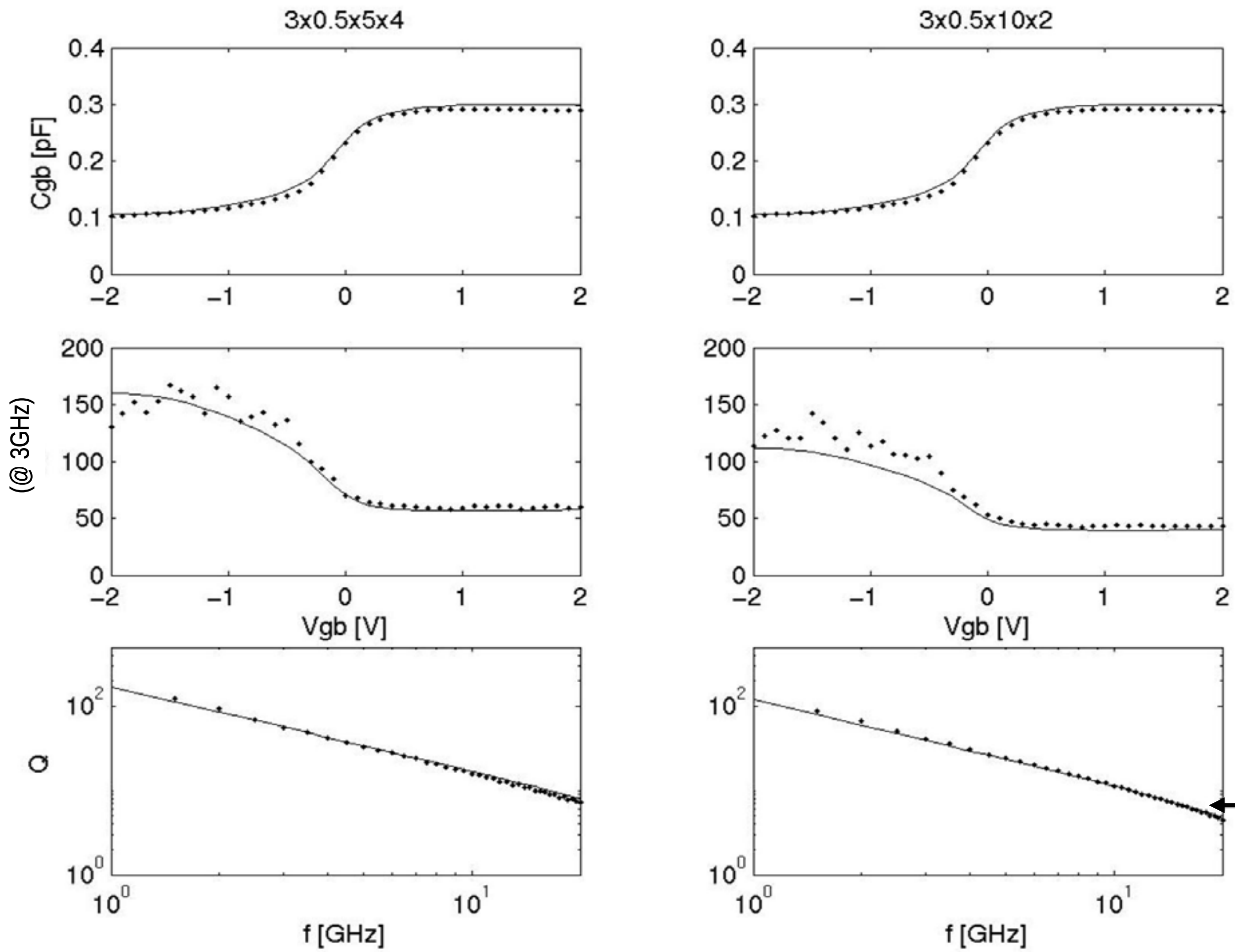
R_{nw} ↑

MOS Varactor Model Results: Varying Wg (0.18 RFCMOS 1.8V Device)



MOS Varactor Model Results: Varying NsxNf (0.18 RFCMOS 1.8V Device)

→ M1 Length



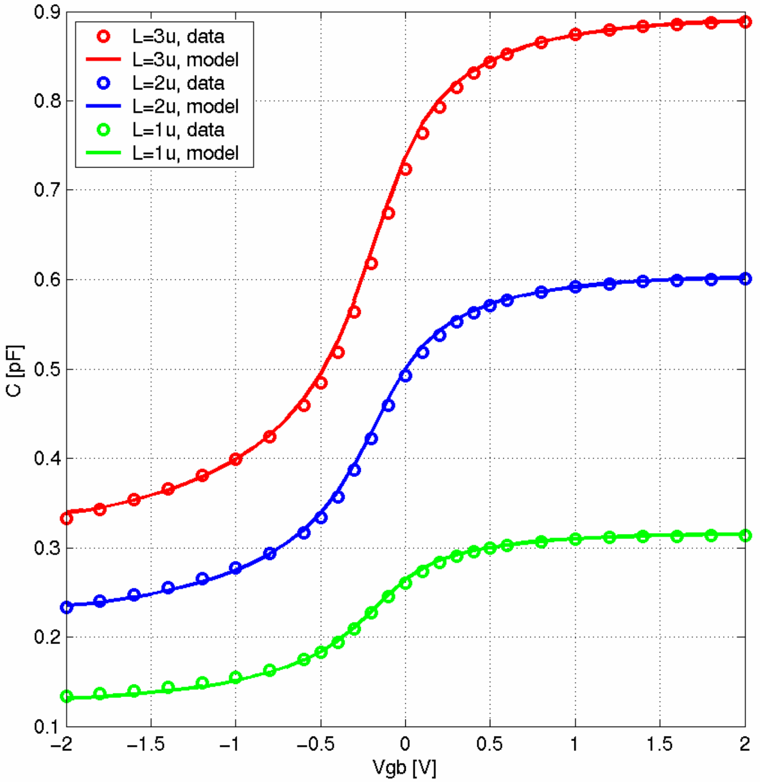
C_{max}/C_{min} —

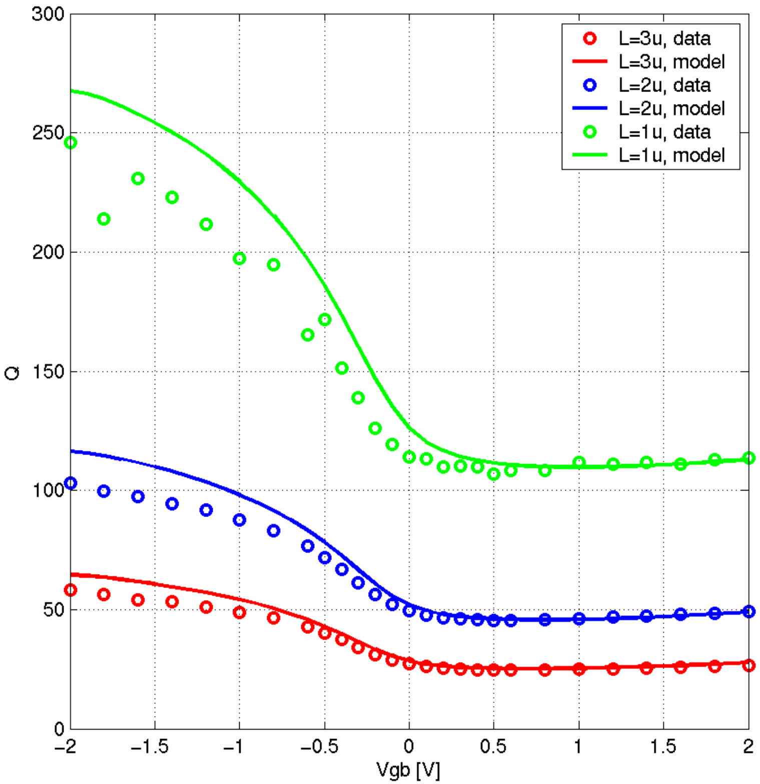
Q ↓

R_{m1} ↑

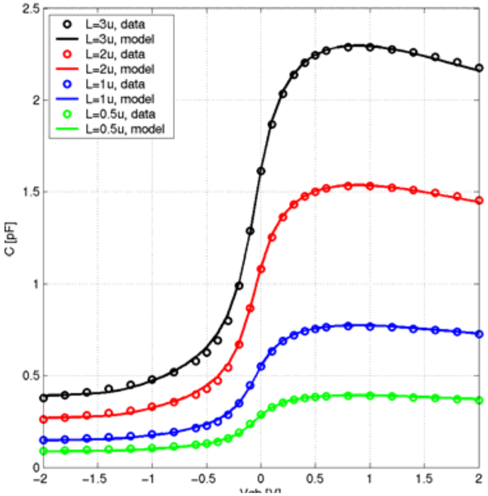
L_g/L_s ↑

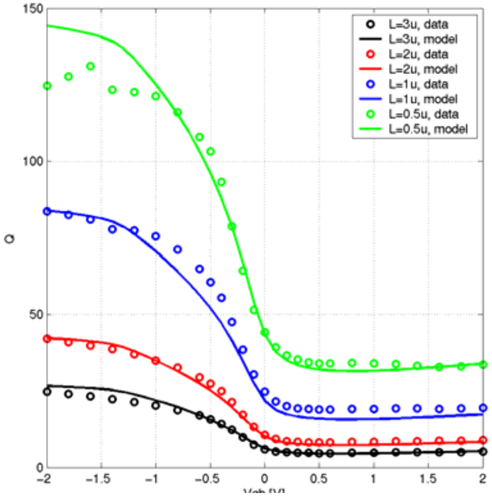
MOS Varactor Model Results: 0.18 RFCMOS, 3.3V Device

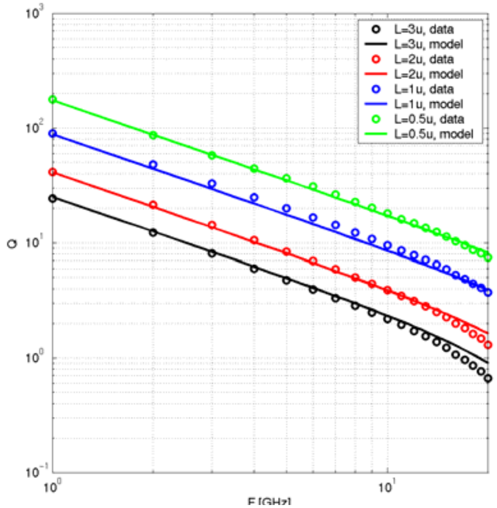


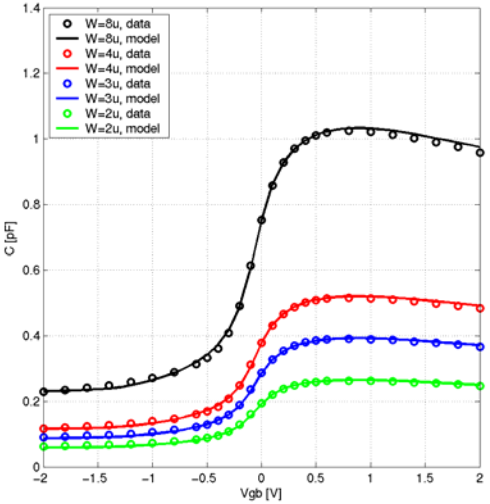


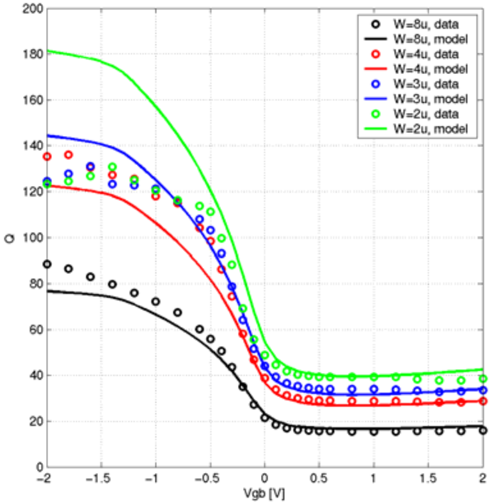
MOS Varactor Model Results: 0.13 RFCMOS, 1.2V Device

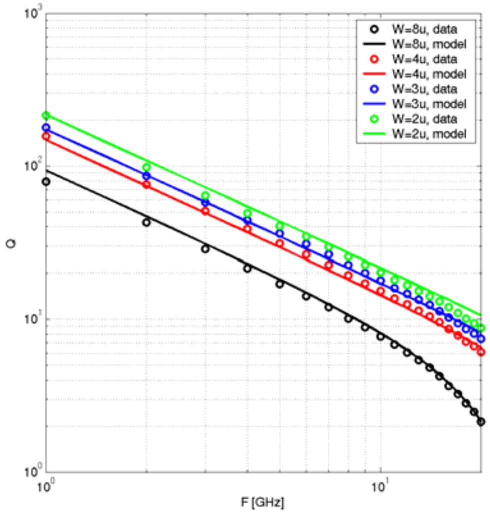






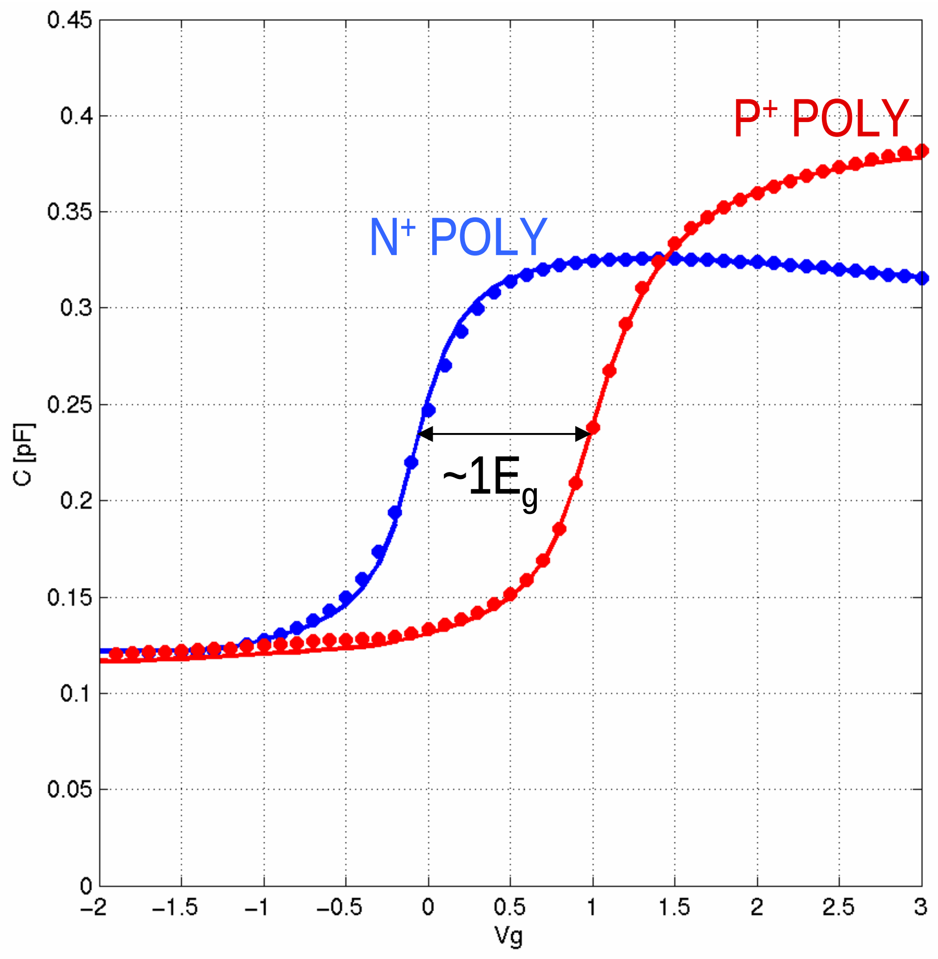






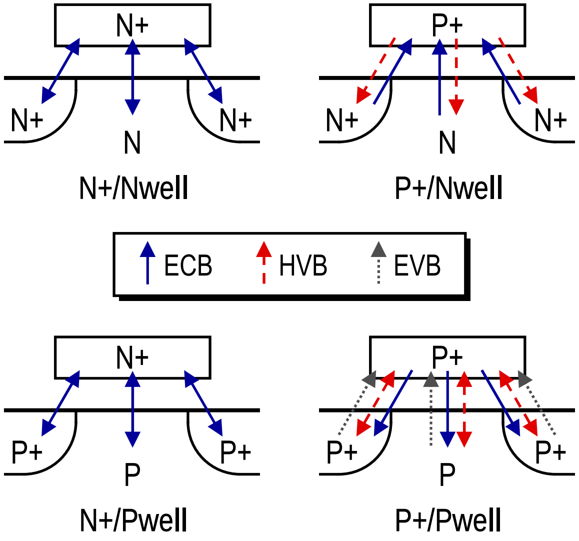
N^+ vs. P^+ Poly MOS Varactors

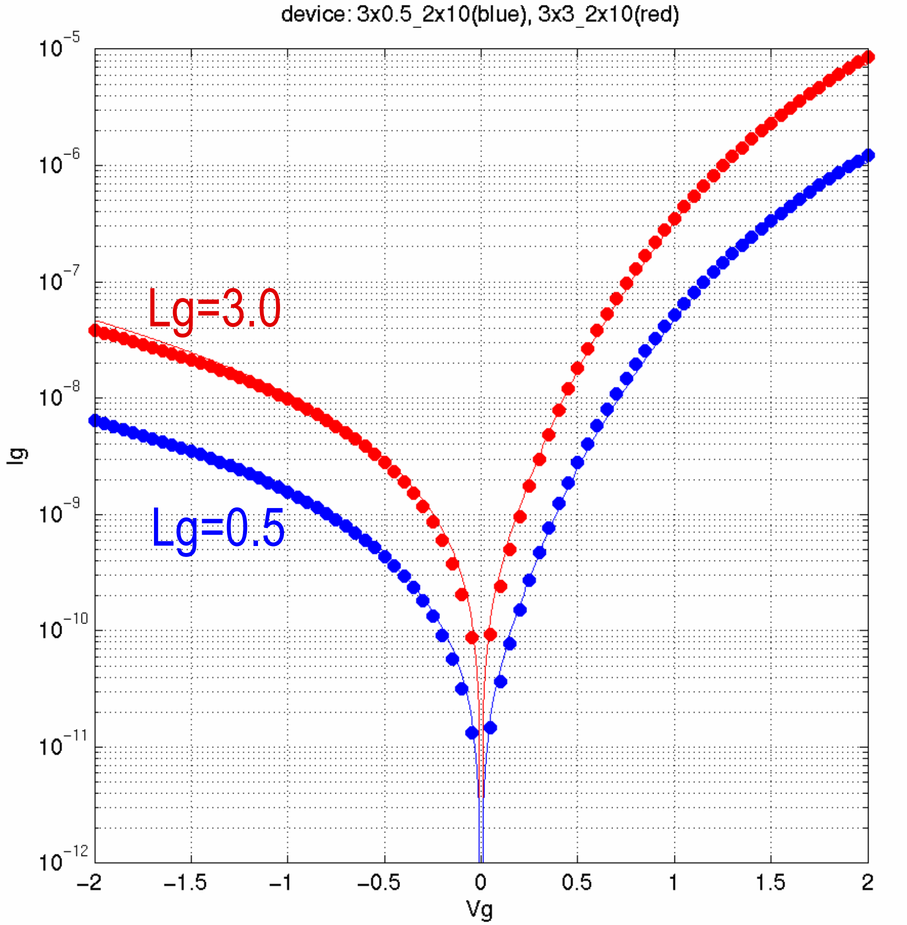
- N^+ poly on Nwell by self-alignment allows for shortest Lg
  - Highest Q
  - Typical VCO biasing requires DC shift of tank voltage to allow for full tuning
  - Easy integration
- P^+ poly on Nwell provides entire tuning range on $+V_{GB}$ axis
  - N^+ contact to Nwell pulled back to prevent counter doping of poly
  - Lg > Lmin to allow to avoid design rule violations in implanting poly with P^+
  - Increases Q minimally
  - Tricky integration but doable



Gate Current

- Accurate modeling of overlap and intrinsic gate current components specific to MOS Varactor structure
- 130nm and below, Ig represents non negligible loss mechanism





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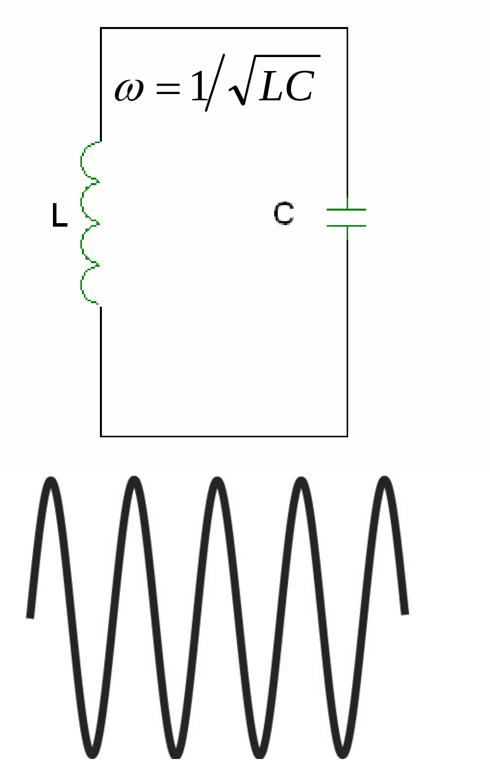
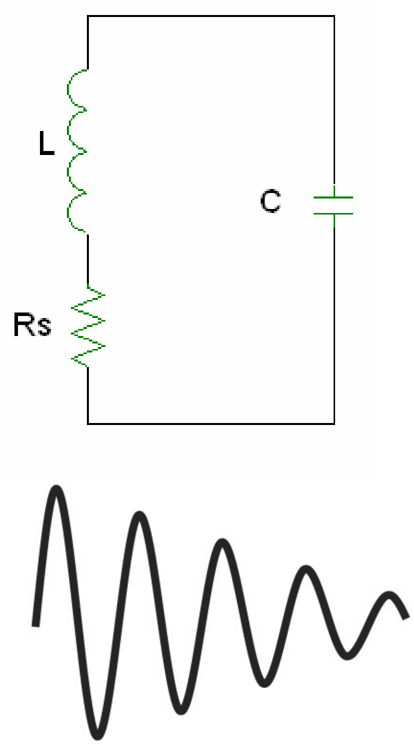
MOS Varactor Effects on Voltage Controlled Oscillator (VCO)

VCO Principles

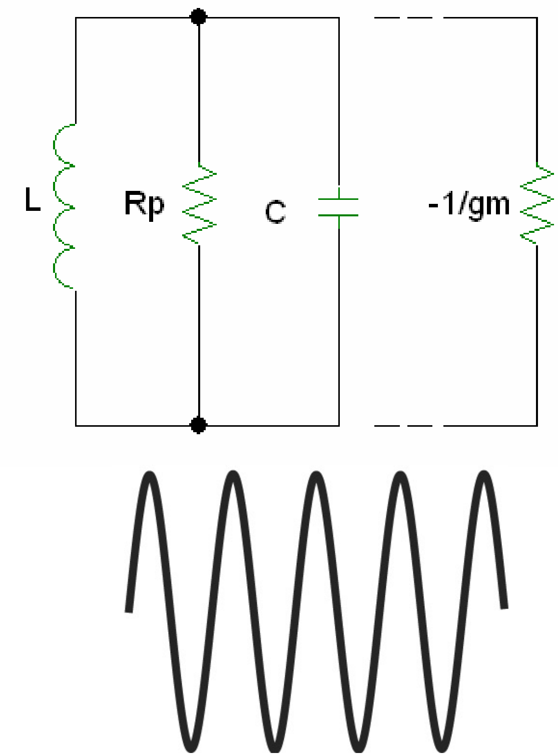
- Ideal Tank Circuit
- Perfect transfer of energy between L&C



- Lossy Tank Circuit
- Energy dissipated in Rs



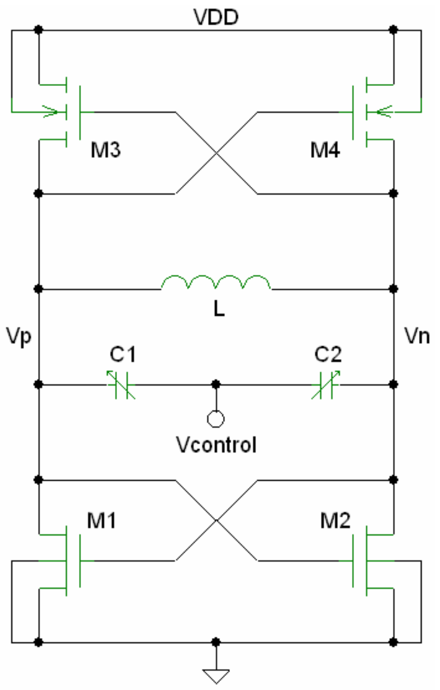
- VCO Tank Circuit
- Energy dissipated in tank compensated by active transistors

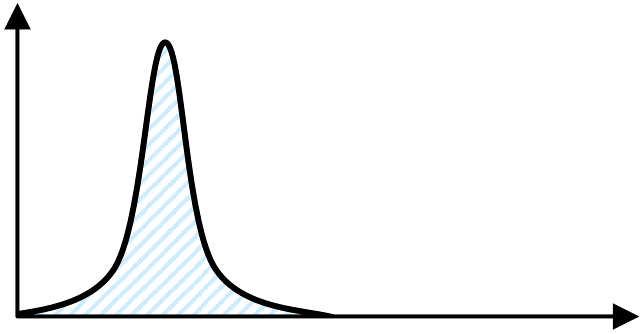


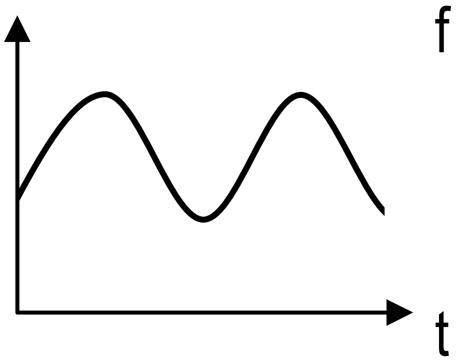
MOS Varactor Purpose: Tune Frequency in VCO

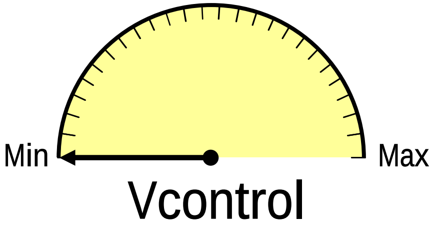
RFCMOS VCO

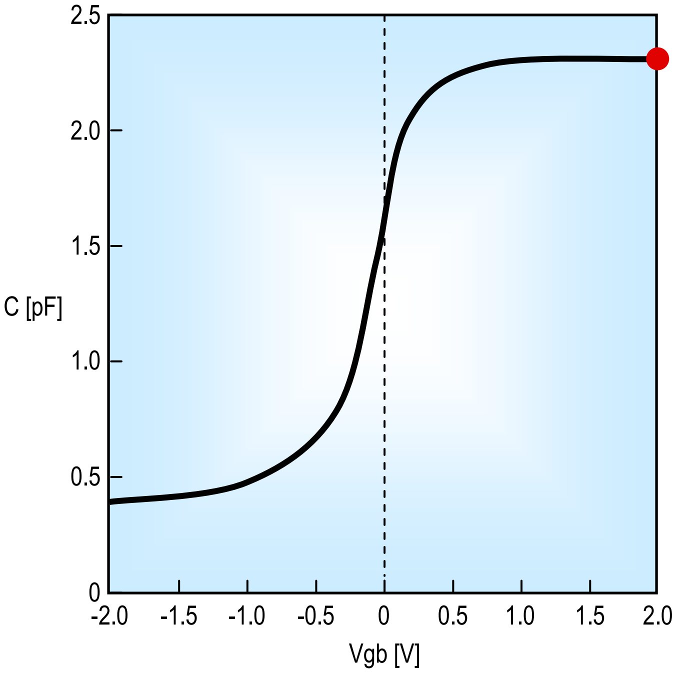
M1/M2 presents -1/gm











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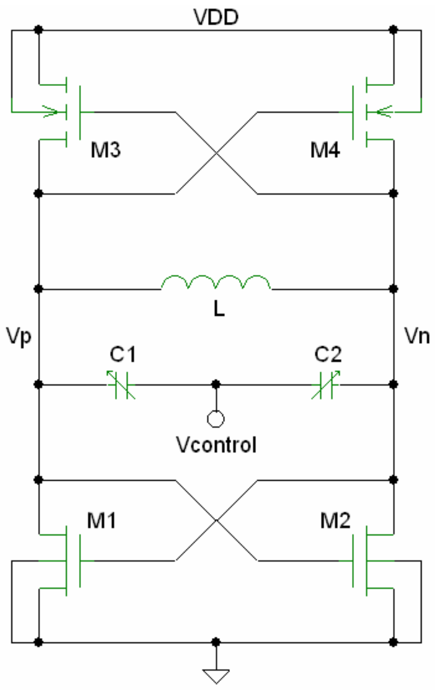

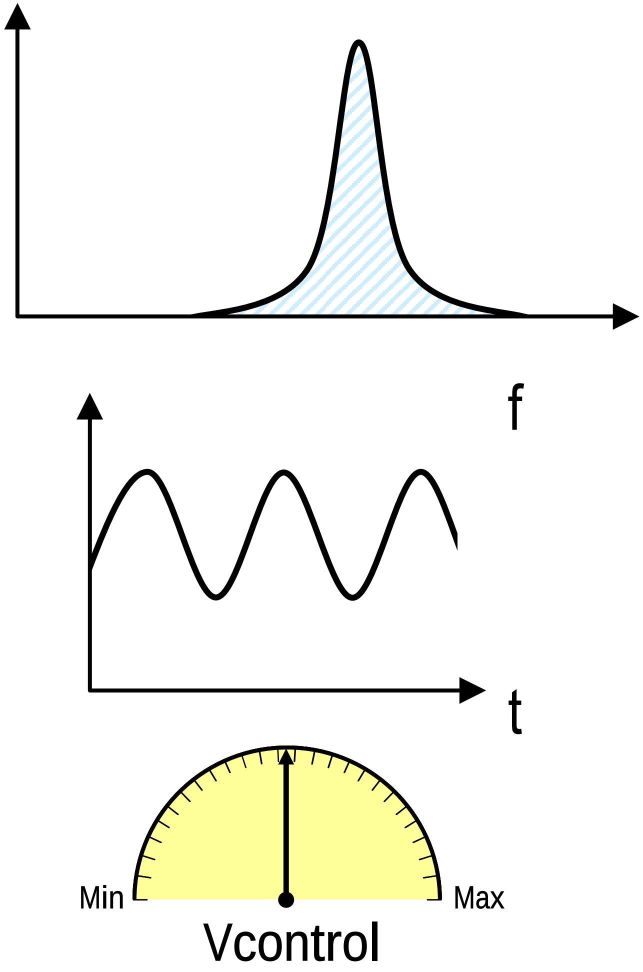

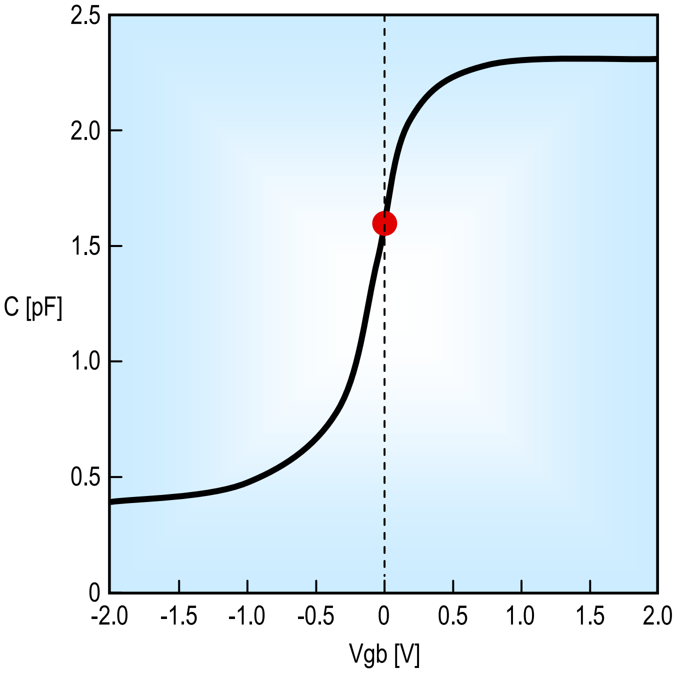

MOS Varactor Purpose: Tune Frequency in VCO

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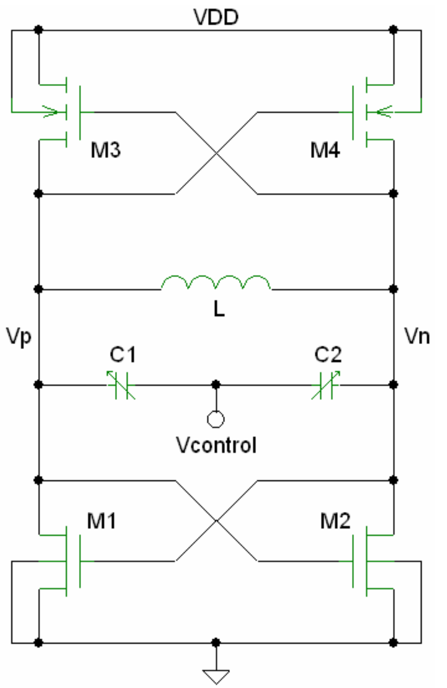
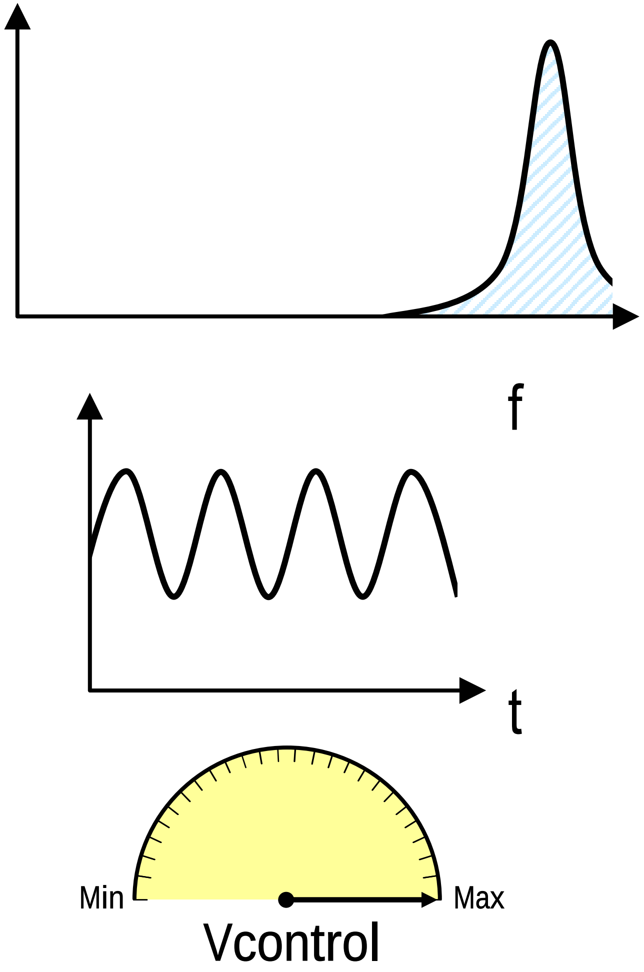
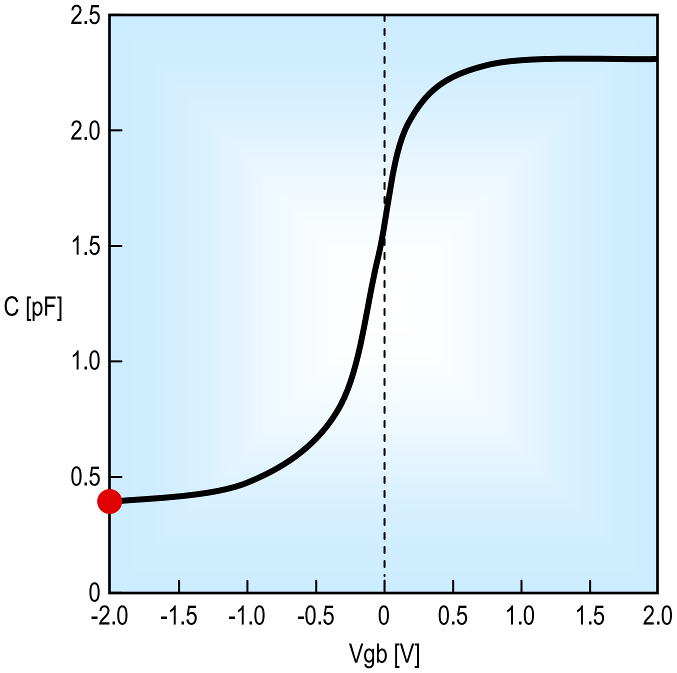


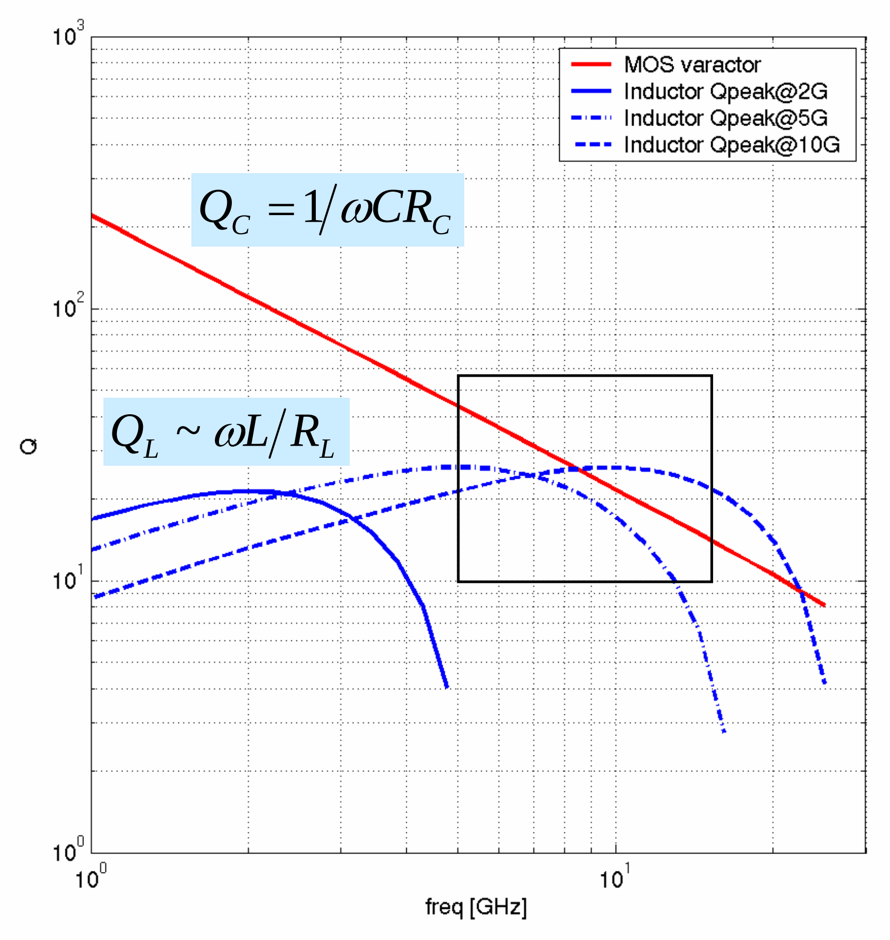




Tank Q: MOS Varactor Influence

$$Q_{tank} = \frac{Q_L \cdot Q_C}{Q_L + Q_C} = \frac{\omega L}{R_L + \omega^2 LCR_C}$$

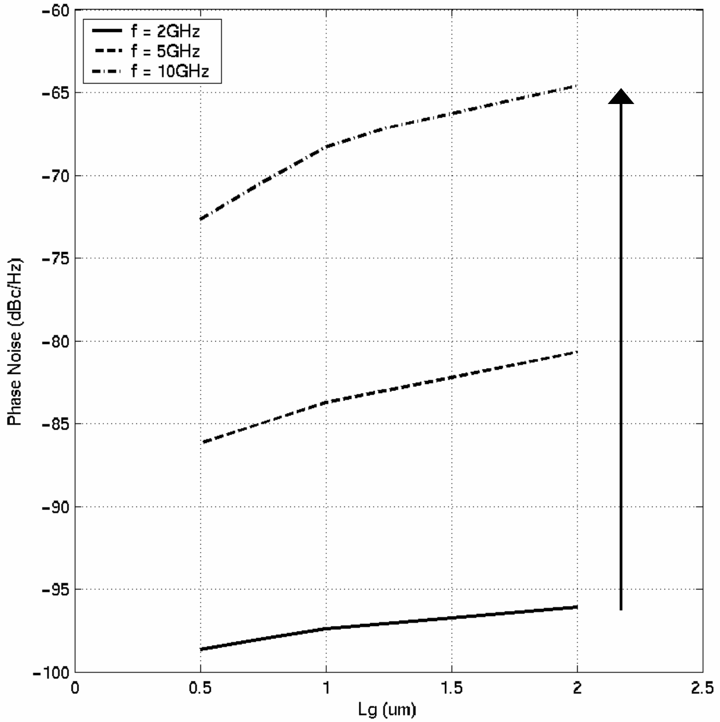
- As frequency increases, varactor Q plays increased role
- Above 5G, MOS varactor Q starts to influence
- Above 10G, MOS varactor Q dominates



MOS Varactor Model Scaling: Phase Noise

$$|H(j\Delta\omega)|^2 = \frac{1}{4(Q_{tank})^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2$$

$$Q_{tank} = \frac{Q_L \cdot Q_C}{Q_L + Q_C} = \frac{\omega L}{R_L + \omega^2 LCR_C}$$

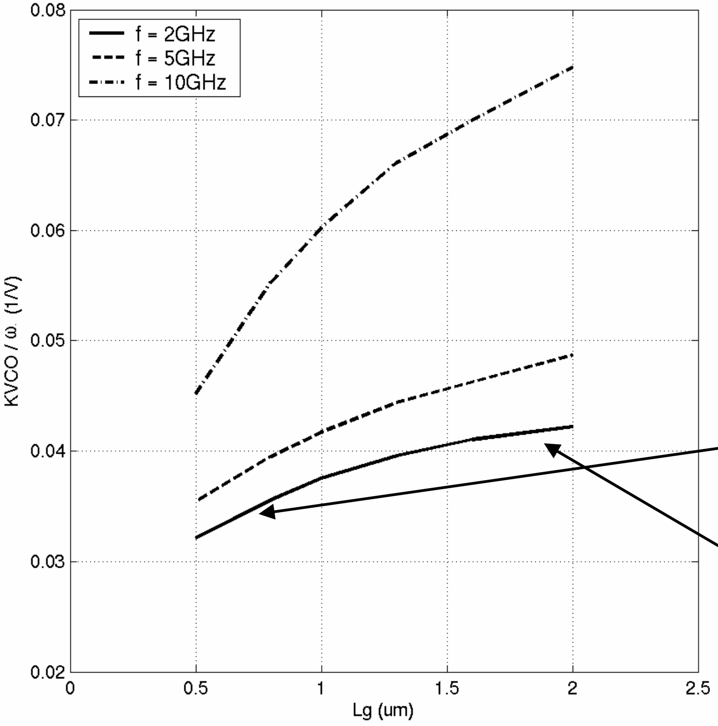


$$|H(j\Delta\omega)|^2 \propto (R_C)^2$$

$$dPN/dLg \uparrow$$

MOS Varactor Model Scaling: VCO Gain

$$KVCO = \left|\frac{d\omega}{dV}\right| = \frac{\omega}{2}\frac{Lg}{\left(C_i' \cdot Lg + C_{FRW}\right)} \cdot \frac{dC_i'}{dV}$$



$$\omega = 1/\sqrt{LC}$$

$$C = C_i' \cdot W_g \cdot L_g + 2 \cdot \mathrm{CFRW} \cdot W_g$$

$$\frac{dC}{dV} = \frac{dC_i'}{dV} \cdot W_g \cdot L_g$$

Small L_g

$$KVCO = \frac{\omega}{2} \cdot \frac{L_g}{\mathrm{CFRW}} \cdot \frac{dC_i'}{dV}$$

Large L_g

$$KVCO = \frac{\omega}{2 \cdot C_i'} \cdot \frac{dC_i'}{dV}$$

Summary MOS Varactor Model: Key Things to Get Right

- Physical CV equation dependent on process and geometry parameters
  - Cmax/Cmin, tuning range variation with geometry
  - Accurate dC/dV critical for VCO phase noise
  - Facilitates accurate statistical modeling
- Accurate models for device resistance over geometry
  - Provides designer ability to trade off tuning range for Q, effectively trading VCO gain vs. phase noise
- Proper dependence of metal parasitics on device layout
  - Poor layout can kill Q
- Gate Current – non-negligible at 130nm and below

References

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