

# A Fractional-N Sigma-Delta Synthesizer with Bipolar-MOSFET Charge-Pump (BiFET CP) for Base-Station Applications

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**Abstract** — With the increasingly demanding for PLL synthesizer very fast locking in base-station applications [1], we have developed a fractional-N sigma-delta synthesizer to validate the newly proposed Bipolar-MOSFET Charge-Pump (BiFET CP). The BiFET CP has been designed by using vertical PNP bipolar devices Jazz’s SiGe60 BiCMOS offered to replace the conventional PFETs in current steering charge pumps. The CP presents three features of small die size, low power consumption, and source-sink current well-matching, which quite fits the CP array design in the synthesizer very fast locking application. The in-band phase noise mainly depending on the CP is tested with  $\sim 105\text{dBc/Hz}$  through whole frequency band (806–853MHz). The synthesizer with VCO integrated in a single-chip has been also fabricated and tested. The phase noise achieved is about  $-145\text{dBc/Hz}$  at 1MHz offset. The total synthesizer has presented very promising performance for base-stations such as GSM.

**Index Terms** — BiFET, charge pump, vertical PNPs, fractional-N synthesizer, fast lock, GSM base-station.

## I. INTRODUCTION

Fractional-N synthesizer is offering fast locking capacity to wireless communications. GSM & EDGE base-stations require synthesizers to be able to hop over full TX or RX band in  $<10\mu\text{s}$  and also have very low phase noise and spurious. The recent progress in the fast locking fractional-N sigma-delta synthesizer can meet the GSM & EDGE requirement by using 64 identical 0.25mA charge pump cells to switch the current for bandwidth control [1]. The charge pump array is demanding its each cell with small-size, power-saving and source-sink current well-matching. The fast locking could be a replacement for the existed solution with twin-synthesizer “ping-pong” switching.

In this paper, we have designed a fractional-N sigma-delta synthesizer to advance its fast-locking feature comparing with integer-N synthesizers. With the design consideration, we have proposed a novel BiFET charge pump with vertical PNP bipolar devices instead of the conventional PFET versions. The BiFET CP targets to small size, low power consumption and source-sink current well-matching for the fast-locking need. The fractional-N sigma-delta synthesizer validates the BiFET CP’s potential advantage with its performance at GSM band.

## II. BIFET CHARGE PUMP

We have used vertical PNP bipolar devices to replace conventional PFETs in current steering charge pumps. The vertical PNP is offered in Jazz’s SiGe60 SBC35QTD 0.35um BiCMOS process [2]. Where the vertical PNP has much higher performance than the passive-like lateral PNP device as shown in the table I.

Besides the vertical PNP, this four-metal layer process also offers active devices of NPN bipolar transistor and 0.35um MOSFET, and passive devices of inductor, capacitor, PN/MOS varactor and resistor.

TABLE I. VERTICAL PNP’s PERFORMANCE

Parameter	Typ.	Units
Beta ( $I_c=10\mu\text{A}$ )	70	
$V_{be}$ ( $I_c=1.4\mu\text{A}$ )	-0.7	V
$V_a$ ( $I_b=10\mu\text{A}$ )	-18	V
$BV_{ceo}$	-7.5	V
$BV_{ebo}$	5	V
$BV_{cbo}$	8	V
Peak $F_t$ ( $V_{ce}=-5\text{V}$ )	17.5	GHz
$J_c$ @ peak $F_t$	0.7	$\text{mA}/\mu\text{m}^2$
Peak $F_{max}$ ( $V_{ce}=-5\text{V}$ )	23.5	GHz
$C_{be}$ ( $V_{be}=0\text{V}$ )	28.4	fF
$C_{bc}$ ( $V_{bc}=0\text{V}$ )	34	fF
$C_{cs}$ ( $V_{cs}=0\text{V}$ )	50	fF
Note: $0.8\times 5\mu\text{m}^2$ emitter with double bases		

We have designed the BiFET CP as shown in the Fig.1. Basic idea is to replace PFETs with vertical PNPs in the current steering architecture. Considering the charge pump principle, we target to well-matching  $U/U_b$  with  $D/D_b$ , where  $U/U_b$  and  $D/D_b$  are differential up/down pulse signals coming from phase detector respectively. Since vertical PNPs have much faster response than MOSFETs, the  $U/U_b$  signal can be immediately transferred to match  $D/D_b$  at the output through “infinite-fast” vertical PNPs. There is least delay happened with  $U/U_b$  matching  $D/D_b$ .

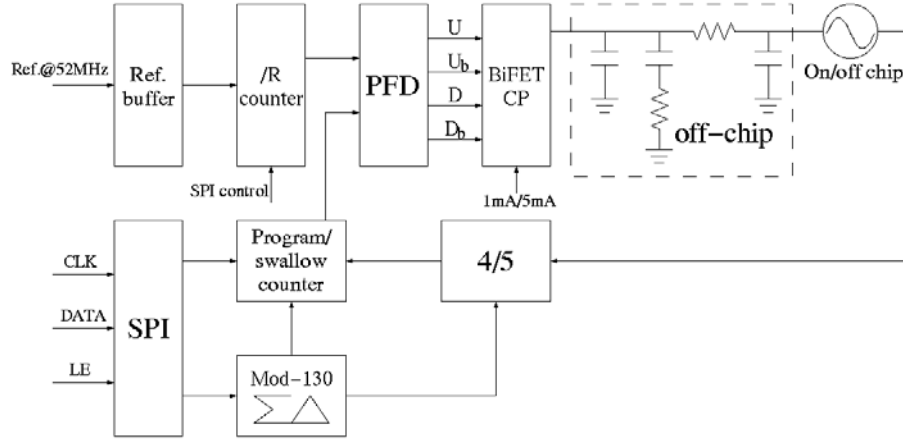


Fig.2. Block diagram in the fractional-N synthesizer

The match between source and sink current therefore depends on how well  $M_1$  &  $M_2$  matching with  $M_3$  &  $M_4$ .  $M_1 \sim M_4$  are kept same dimensions of  $0.35\mu\text{m}$  length,  $14\mu\text{m}$  width and 8 fingers. We have used three cascaded current sources with  $5\text{mA}/1\text{mA}$  operation modes in the charge pump to enhance the matching impedance. The vertical PNP has been chosen with double-emitter size of  $0.8\mu\text{m} \times 10\mu\text{m}$  for the  $5\text{mA}$  mode and single-emitter size of  $0.8\mu\text{m} \times 5\mu\text{m}$  for the  $1\text{mA}$  mode to dynamically bias the PNP at higher  $f_T$  during the operation.

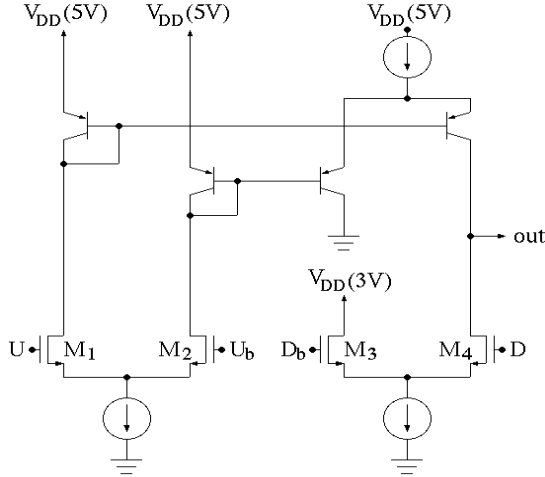


Fig. 1. BiFET CP schematic.

### III. FRACTIONAL-N SYNTHESIZER

Fig.2 shows synthesizer function blocks on the closed loop path. The VCO output signal goes through prescaler and programmable/swallow counters to compare with reference signal through reference buffer and R divider at the PFD input port. The PFD detects phase difference between the reference signal and the VCO generated to output  $U_p/D_n$  differential voltage pulses into the BiFET

CP. The differential voltage pulse signal is converted into current pulses by the BiFET CP to charge /discharge the low pass filter off-chipped and tune the VCO's output frequency reaching lock conditions. In test, we have setup R-counter  $\div 2$  and divided the reference signal of  $52\text{MHz}$  into  $26\text{MHz}$ . The prescaler is designed with  $4/5$  modulus. The 3<sup>rd</sup> mesh sigma-delta modulator randomizes the  $4/5$  modulus to shape the quantization noise to high frequency band and meanwhile realize the fractional function. The SPI has been designed for channel and block function controls such as current mode switching in the BiFET CP.

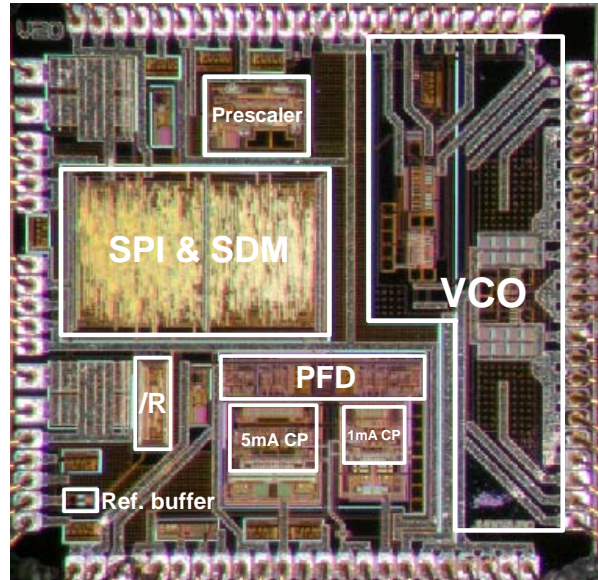


Fig. 3. Die photo.

Fig.3 shows the die photo with different function blocks nominated. This fabrication has total die size of  $2.35 \times 2.35\text{mm}^2$  and integrates the synthesizer with VCO in

a single-chip. The BiFET CP has been laid out with  $\sim 0.06\text{mm}^2$  for the 5mA mode and  $\sim 0.03\text{mm}^2$  for 1mA mode. The layout has included the CP core and current mirror circuitry ready to connect with bandgap/PTAT current output. In the photo, wide metals grounded cross between function blocks for isolations, particularly the isolation between digital blocks and analog/RFs.

#### IV. TEST RESULTS AND DISCUSSION

We have discussed the small-sizing feature. The low power consumption and source-sink current well-matching are another two features left. Fig.4 shows the source-sink current variation with charge pump output voltage connected to low pass filter off-chipped in the chip test. With the 5V supply, we assume the tuning range 0.5V~3.5V to see if we could achieve source-sink current well-matching and low phase noise qualified at the in-band frequency test. According to the common used symmetric description, we can define  $I_{\text{DOMT}}$  and  $I_{\text{DOVD}}$  in equation (1) and (2) to characterize the current symmetry.

$$I_{\text{DOMT}} = (||I_3|-|I_4||) / [(|I_3|+|I_4|)/2] \times 100\% \quad (1)$$

$$I_{\text{DOVD}} = [(||I_2|-|I_1||) / 2] / [(|I_1|+|I_2|) / 2] \times 100\% \quad (2)$$

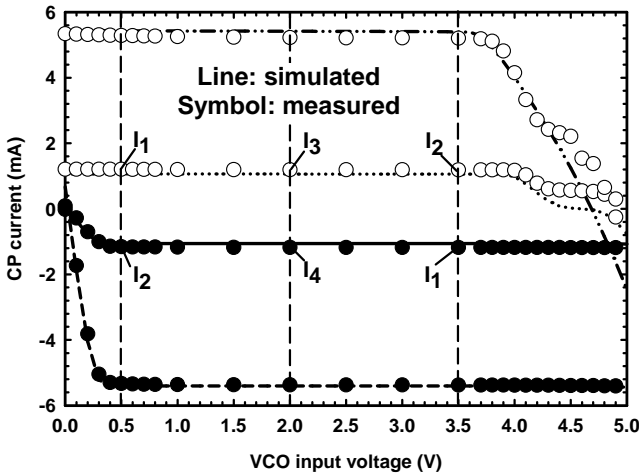


Fig. 4. BiFET CP's source-sink current matching with Vtune.

Table II has shown the source-sink current symmetry. The current has well-matching features through 0.5V~3.5V tuning voltage range. The whole chip test also presents in-band phase noise of  $\sim -105\text{dBc/Hz}$  through the whole tuning range as the shown in Fig.5. Since the BiFET CP could directly realize the differential to single-ended conversion instead of the additional conversion amplifier. The CP saves the high conversion current (30mA in [1]) and only operates with low bias current of 1~2mA and

CP's source-sink currents. Besides the conversion power saving, since the vertical PNP bipolar device has breakdown voltages higher than the 5V supply while 0.35um PFETs can only stand 3.3V, the BiFET CP can thus save additional protection circuits such as the common-mode feedback in PFET CPs and further save the additional protection power and die size.

TABLE II. CURRENT MATCHING TESTED

Parameter	IDOVD (%)		IDOMT (%)	
	1mA	5mA	1mA	5mA
Source	0.67	0.78	1.09	2.76
Sink	0.98	0.45		

The whole synthesizer has been also tested. Phase noise can be characterized with  $-146\text{dBc/Hz}$  at 1MHz offset frequency when the VCO oscillates at 853MHz (Fig.6a). Through 45MHz bandwidth, the phase noise can measure  $\sim -145\text{dBc/Hz}$  level at 1MHz offset (Fig.6b). The whole synthesizer performance has been summarized in Table III. Even the settling time we have achieved is 460us that can satisfy GSM base station requirements in the existed twin-synthesizer "ping-pong" switching solution, the fractional-N synthesizer still has potential features to achieve the very fast lock solution. We have tested the spur performance by using separate two chips, one using PLL and another one using VCO for good isolations. In the single chip integrated PLL with VCO, the spur can achieve  $-72\text{dBc}$  @600KHz rather than  $-86\text{dBc}$  @600KHz as the Table III shown. This means the fractional-N synthesizer can achieve much better spur isolations with VCO off-chipped than the on-chipped. The BiFET CP costs very low current due to the vertical PNP applied. The chip size has already included the VCO. The total synthesizer presents very promising performance for base-station applications such as GSM.

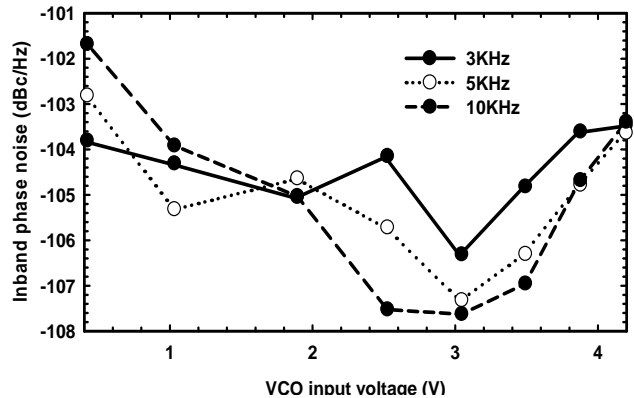


Fig. 5. In-band phase noise measured with Vtune.

TABLE III. SUMMARY OF PERFORMANCE

Parameter	Typical	Units	Conditions
RF input range	0.5~1.3	GHz	-15~0dBm
RMS phase error	0.6	Degree	Over 577us time lot
Settling time	460	us	Within phase error accuracy
RF output power	~ 6.0	dBm	50ohm load
CP: Current source	$\pm 1.0/\pm 5.0$	mA	Source-sink symmetry
Bias current	1~2	mA	
Chip size (1mA/5mA)	~ 0.03/~ 0.06	mm <sup>2</sup>	Core with mirror bias circuitry
Phase noise	~ -105	dBc/Hz	In-band over bandwidth
	~ -145	dBc/Hz	@ 1MHz offset over bandwidth
Spurs	-65	dBc	@ 200KHz with VCO off-chipped
	-76	dBc	@ 400KHz with VCO off-chipped
	-86	dBc	@ 600KHz with VCO off-chipped
	-72	dBc	@ 600KHz with VCO on-chipped
Chip size	2.35x2.35	mm <sup>2</sup>	VCO integrated
Technology	0.35	um	Jazz's SiGe60 BiCMOS
Package	5x5	mm <sup>2</sup>	28 lead QFN

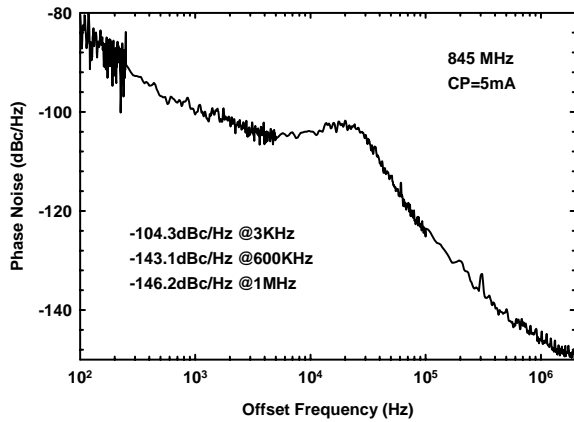


Fig. 6a. SSB phase noise measured at 845MHz.

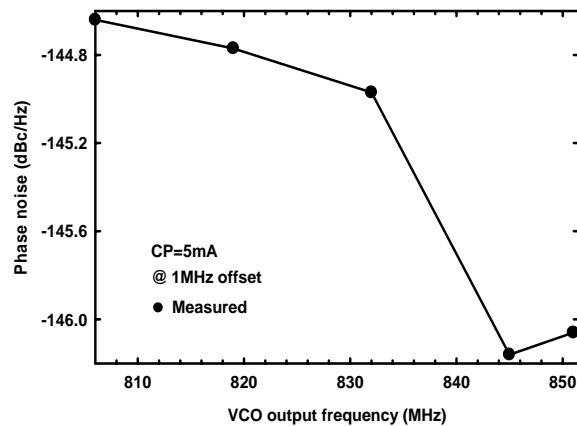


Fig. 6b. Phase noise measured through 45MHz bandwidth.

## V. CONCLUSION

We have developed a fractional-N sigma-delta synthesizer with BiFET CP for GSM base station applications. The BiFET CP has been designed by using the vertical PNP bipolar device to replace the conventional PFET in current steering charge pump. The CP presents small-sizes of  $\sim 0.06\text{mm}^2$  for the 5mA mode and  $\sim 0.03\text{mm}^2$  for 1mA mode, low-power consumption with 1~2mA bias current and 1mA/5mA source current, and source-sink current well-matching with the in-band phase noise of  $\sim 105\text{dBc/Hz}$ . The designed synthesizer has been tested with the low phase noise of  $\sim 145\text{dBc/Hz}$  through 45MHz wider bandwidth at 1MHz offset. The total synthesizer has achieved very promising performance for base-stations such as GSM. The BiFET CP validated in the synthesizer with small-sizing, power-saving and current well-matching fits the CP array design in very fast locking applications.

## ACKNOWLEDGEMENT

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